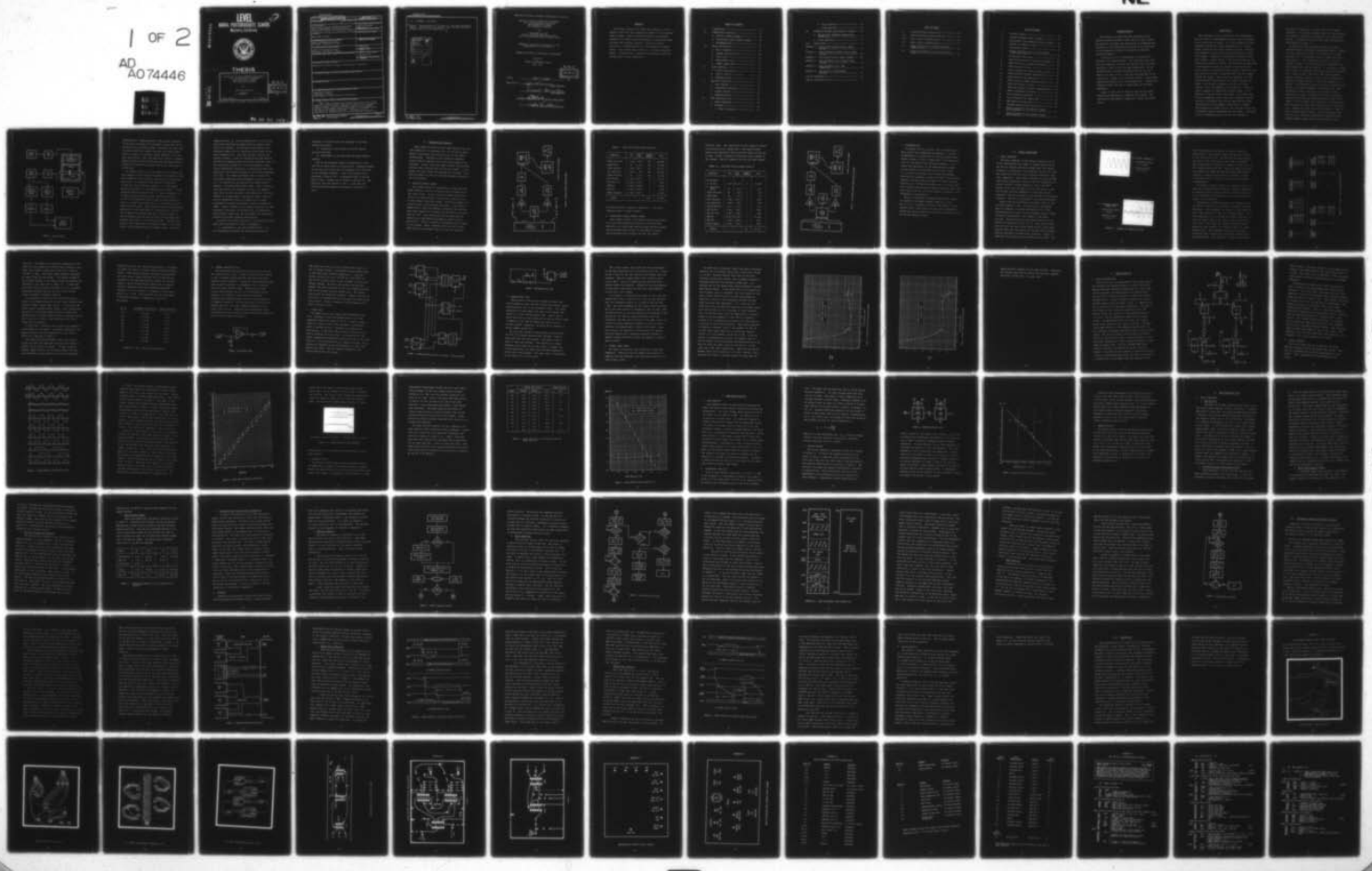
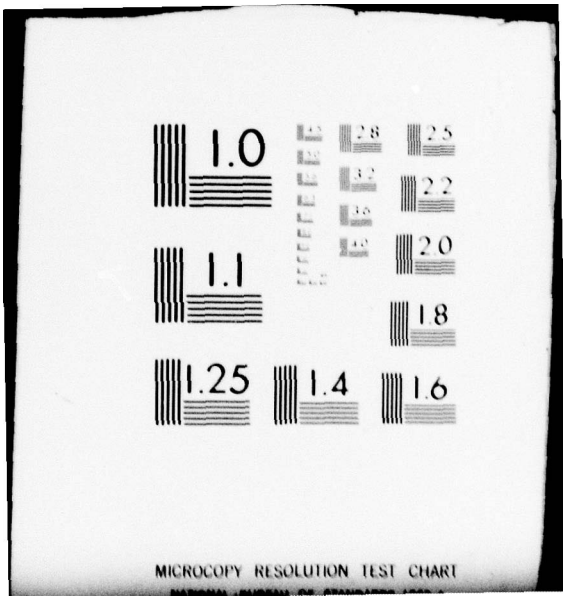
AD-A074 446 NAVAL POSTGRADUATE SCHOOL MONTEREY CA F/G 9/2
ANALOG AND DIGITAL HARDWARE DEVELOPMENT FOR A MICROCOMPUTER CON--ETC(U)
JUN 79 R O CARLOCK

UNCLASSIFIED NL

1 OF 2
AD A074446




1.0
1.1
1.25
1.4
1.6
2.0
2.2
2.5
1.8
MICROCOPY RESOLUTION TEST CHART

# LEVEL II

# NAVAL POSTGRADUATE SCHOOL

## Monterey, California

(9) Master's THESIS

(6) ANALOG AND DIGITAL HARDWARE DEVELOPMENT FOR A MICROCOMPUTER CONTROLLED DATA ACQUISITION SYSTEM FOR ACOUSTICAL IMAGING.

by

(10) Reid Owen Carlock

(11) June 1979 (12) 98 p.

Thesis Advisor: J. P. Powers

Approved for public release; distribution unlimited.



251 450

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

| REPORT DOCUMENTATION PAGE | | READ INSTRUCTIONS BEFORE COMPLETING FORM |
|---|---|---|
| 1. REPORT NUMBER | 2. GOVT ACCESSION NO. | 3. RECIPIENT'S CATALOG NUMBER |
| 4. TITLE (and Subtitle)<br>Analog and Digital Hardware Development for a Microcomputer Controlled Data Acquisition System for Acoustical Imaging | | 5. TYPE OF REPORT & PERIOD COVERED<br>Master's thesis; June 1979<br>6. PERFORMING ORG. REPORT NUMBER |
| 7. AUTHOR(s)<br>Reid Owen Carlock | | 8. CONTRACT OR GRANT NUMBER(s) |
| 9. PERFORMING ORGANIZATION NAME AND ADDRESS<br>Naval Postgraduate School<br>Monterey, California 93940 | | 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS |
| 11. CONTROLLING OFFICE NAME AND ADDRESS<br>Naval Postgraduate School<br>Monterey, California 93940 | | 12. REPORT DATE<br>June 1979<br>13. NUMBER OF PAGES<br>97 |
| 14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) | | 15. SECURITY CLASS. (of this report)<br>Unclassified<br>15a. DECLASSIFICATION/DOWNGRADING SCHEDULE |

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Acoustical Imaging
Underwater Viewing
Microcomputer Controlled Data Acquisition

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This thesis presents the design and testing of a microcomputer controlled data acquisition system for an acoustical imaging system. Analog sinusoidal signals are processed through a 256 channel analog multiplexer to high speed phase and amplitude detection channels. Analog to digital conversion is accomplished with a microcomputer peripheral

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-014-6601
(Page 1)



UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

(20. ABSTRACT Continued)

module. Data storage then follows in a 64K byte peripheral memory. Interface with a cassette tape recording system is accomplished for data transferral.

| Accession For | |
|---|---|
| NTIS GRA&I | ☒ |
| DDC TAB | ☐ |
| Unannounced | ☐ |
| Justification | |
| By | |
| Distribution/ | |
| Availability Codes | |
| Dist. | Avail and/or special |
| A | |

Approved for public release; distribution unlimited.

# Analog and Digital Hardware Development for a Microcomputer Controlled Data Acquisition System for Acoustical Imaging

by

Reid Owen Carlock
Major, United States Marine Corps
B.S., United States Naval Academy, 1968

Submitted in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL

June 1979



Author Reid O Carlock

Approved by: John S Powers
Thesis Advisor

Rudolf Panholzer
Second Reader

W R Kirk
Chairman, Department of Electrical Engineering

William M Tolles
Dean of Science and Engineering

## ABSTRACT

This thesis presents the design and testing of a microcomputer controlled data acquisition system for an acoustical imaging system. Analog sinusoidal signals are processed through a 256 channel analog multiplexer to high speed phase and amplitude detection channels. Analog to digital conversion is accomplished with a microcomputer peripheral module. Data storage then follows in a 64K byte peripheral memory. Interface with a cassette tape recording system is accomplished for data transferral.

TABLE OF CONTENTS

## LIST OF TABLES

## LIST OF FIGURES

## ACKNOWLEDGEMENT

This material is based upon work supported by the National Science Foundation under Grant No. Eng 77-21600. Any opinions, findings, and conclusions or recommendations expressed in this publication are those of the author and do not necessarily reflect the views of the National Science Foundation.

I would also like to acknowledge the guidance and patience of my thesis advisor. His tolerance of my trial and error approach to design and testing, which oft times resulted in loss of time, was much appreciated. He was concerned that I achieve the stated objective of this thesis, but more so that I have and take advantage of the opportunity to learn. As a military officer, I have always appreciated working with a true professional. Working with Professor Powers has been an educational and enjoyable experience.

Lastly I would like to thank my wife for her understanding and assistance in preparing this thesis. Her contribution was personal, supportive, needed and always there.

# I. INTRODUCTION

Wave phenomena, such as diffraction and interference, are not unique to electromagnetic waves; similar phenomena occur with acoustical waves. It is the adherence to these phenomena that permits image reconstruction of a target object insonified with planar acoustical waves. Consider an incremental volume of the target through which a wave-front passes. Depending on the material structure within that volume, a certain degree of the wave's energy will be transmitted through the target. The intensity and amplitude of the transmitted wave will depend on how much of the wave's energy is reflected from the target's surface on the near side and how much is absorbed while the front passes through the target. Recall that the frequency of a wave passing through multiple media will remain constant and equal to the original frequency, but that the "phase velocity" will vary depending on the material's relative density compared to immediately adjacent areas. To an observer on the far side of the target, the surface area of each incremental volume looks like a separate "source" emitting an acoustical wave with an amplitude and phase characteristic of the segment through which it passed. The propagation of waves from all the "sources" sets up an interference pattern downstream from the target. Contained in this interference pattern is all the information

necessary to reconstruct a visual image of the target insonified. This thesis concerns itself with the detection and storage of information contained in the interference pattern. Processing of the data and image reconstruction are presented in Refs. 1-3.

An acoustical imaging system has been an on-going research project at the Naval Postgraduate School. Figure 1 is a very simplified diagram of the system at its most advanced point of development prior to commencing work on this thesis. It will hereafter be referred to as the "original system." The following briefly summarizes the work accomplished with this system. It consists of a water tank housing an acoustical wave source, target and detector unit. Signal source, amplifiers, amplitude and phase detector channels, analog to digital (A/D) conversion and recording equipment external to the tank complete the system. A one megahertz sinusoidal signal is amplified and applied to a planar transducer in the water tank. The interference pattern created by the acoustical waves insonifying a target is detected by a single ultrasonic receiving probe scanning across and down the face of the target. A 64 x 64 sample point matrix can be achieved with each 64 sample line vertically aligned with the preceding line. Samples are taken every half wavelength (.75mm) to obtain optimum sample spacing. As the probe scans from side to side it has been experimentally determined that scanning speeds greater than thirty seconds per line

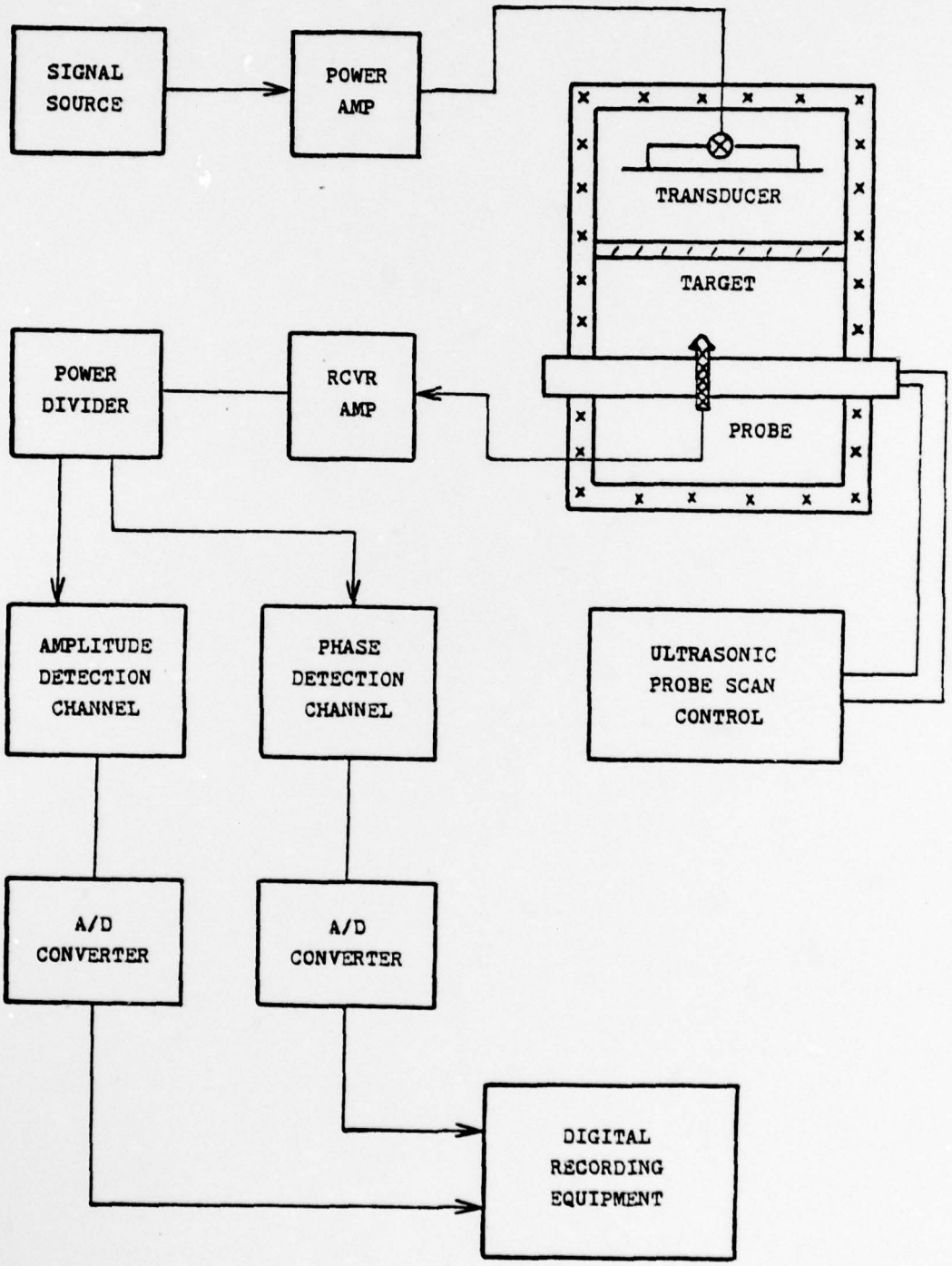



FIGURE 1 - ORIGINAL SYSTEM

(approximately 2 samples/second) create enough turbulence in the water to destroy any meaningful signals that can be detected by the ultrasonic probe. Therefore the total time to collect data for a target less than two inches square takes in excess of 30 minutes, hardly adequate for a real time image system. This scan speed also results in approximately one half second for the amplitude and phase detector channels to produce their analog and digital values and to record them.

The overall objective of this thesis was to improve the time response of the entire data acquisition system for scan areas expanded four to sixteen times the size of previous scan areas. To accomplish this the entire system was divided into four functional blocks: (1) a 256 channel analog multiplexer, (2) the phase detector channel, (3) the amplitude detector channel, and (4) a data processing unit. A linear detector receiving array (aligned vertically) of 128 or 256 detectors would be used to sweep across the face of a target once instead of 128 or 256 times with the single receiver probe. Each detector would be electronically gated open by the multiplexer in a ripple motion from the top at speeds fast enough such that an entire column of 128/256 samples would be taken in the time one sample had formerly been taken in the original system. Then when the detector array completes its horizontal sweep, it will have taken a 128/256 square matrix of sample points. Since the

sampling period, $T_s$, is now reduced from 0.5 s to 2.0 ms, much faster amplitude and phase detector channels would need to be designed. An 8080 based microcomputer with peripheral memory and A/D conversion modules make up the data processing unit. Once data has been obtained and stored in memory, it must be transferred by some means to the PDP-11/50 computer used for further processing (Ref. 2). The input/output capability of the microcomputer chosen allows considerable flexibility in manipulating data once acquired by the working registers of the Central Processing Unit (CPU). For reasons presented later in Section VI, the present system has been programmed to store all data, as it is generated by the amplitude and phase detector channels, in Random Access Memory (RAM). Then a follow up interrupt routine will transfer the data to a cassette tape, which is then available to the PDP-11/50. This data transfer is accomplished in the parallel mode. Data can also be transferred serially by means of an on board programmable universal asynchronous receiver transmitter (UART). Serial transfer via an acoustic coupling link over telephone lines direct to the PDP-11/50 is a possibility. Data transfer schemes are user selectable with appropriate software and minimal hardware modifications.

To achieve the overall objective, the following interim goals were established in order of precedence:

(1) Development of the data processing unit, i.e., its microcomputer software and hardware modifications

necessary to interface with the remainder of the data acquisition system.

(2) Construction and testing of the 256 channel analog multiplexer.

(3) Improvement of the amplitude and phase detector channels.

Much of the equipment needed to attack Goal 1 took from two to three months to be delivered. Untested software was written but further work was postponed until delivery of the necessary equipment. Goal 2 was pursued and is discussed in Section III. As equipment began to arrive, work in Goal 1 resumed and is covered in Section VI. The remaining time was devoted to Goal 3. Work here and difficulties encountered are discussed in Sections IV and V.

## II. SYSTEM DESIGN ANALYSIS

Design specifications for the linear detector have not been submitted to a contractor yet, so work had to begin several steps beyond the starting point in the overall system design. Therefore in all instances hereafter, signals from the detector array have been assumed to be available. Signal levels have been forecast from the best available data obtained from the original system. At the outset, two data acquisition schemes were proposed. This section presents a cost and time effectiveness analysis of the two proposals.

### A. MULTIPLE CHANNEL SCHEME

This scheme called for construction of amplitude and phase detector circuits for each of the 256 detectors of the linear array. Initial work had already produced the nucleus of a phase detector circuit for a nominal $4.00, so this seemed a plausible scheme. This would present 512 analog values to be digitized and stored. Eight memory mapped analog input microcomputer peripheral devices from Burr Brown capable of 64 inputs each (MP 8632-AO) would be used for this. Data manipulation and storage would be handled by an 8080 based microcomputer system (Intel's SBC 80/10A). Figure 2 presents a conceptual block diagram of this scheme. Table I presents cost and time figures. "ETD" stands for estimated time till delivery quoted by

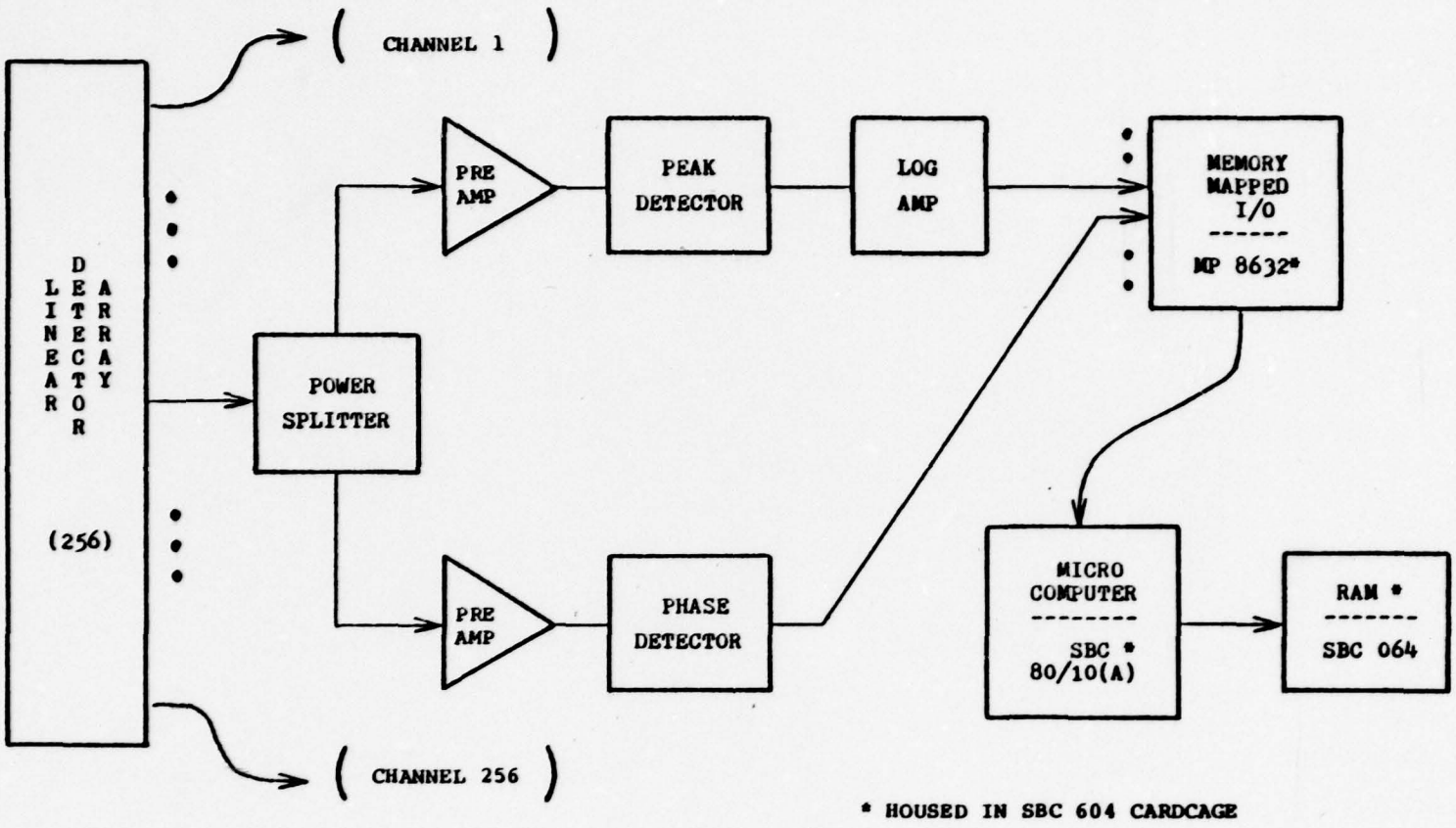



FIGURE 2 - MULTIPLE CHANNEL DETECTOR SCHEME

TABLE I. Cost/Time Effectiveness Study #1

| Component | ETD | Unit Cost | Number Needed | Cost |
|---|---|---|---|---|
| Power splitter | 6 wks | $40 | 255 | $10,200 |
| Amplifiers | IH | @ $3 | 512 | $1,536 |
| Peak Detector | 4 wks | $132 | 256 | $33,792 |
| Log Amplifier | 3 wks | $59 | 256 | $15,104 |
| Phase Detector | IH | @ $4 | 256 | $1,024 |
| MP 8632-AO | 14 wks | $534 | 8 | $4,272 |
| SBC 80/10(A) | 10 wks | $495 | 1 | $495 |
| SBC-064 | 10 wks | $2,200 | 2 | $4,400 |
| SBC-604 | 4 wks | $195 | 3 | $585 |
| Power Supplies | 12 wks | $540 | 3 | $1,620 |
| TOTALS | - | - | 1552 | $73,028 |

by factories making respective components. "IH" means components were "in hand" already.

B. MULTIPLEXED SINGLE CHANNEL SCHEME

This scheme involves a 256 channel analog multiplexing unit that gates through the outputs of the individual detectors to a single amplitude and phase detector channel. The multiplexer would consist of seventeen 16 channel analog switches from Siliconix (DG 506) and channel

selection logic. The latter half of this scheme is similar to the previous one, except that a less sophisticated analog input peripheral device from Burr Brown, MP 8616-AO, is used. Figure 3 presents a conceptual block diagram of this scheme. Table II presents the cost and time figures.

TABLE II. Cost/Time Effectiveness Study #2

| Component | ETD | Unit Cost | Number Needed | Cost |
|---|---|---|---|---|
| Multiplexer | | | | |
| a. DG 506 | 3 wks | $16.36 | 17 | @ $278 |
| b. Selection Logic | IH | @ $5 | 1 | @ $5 |
| Power Splitter | IH | $40 | 1 | $40 |
| Amplifiers | IH | @ $3 | 2 | $6 |
| Peak Detector | 4 wks | $162 | 1 | $162 |
| Log Amplifier | 3 wks | $59 | 1 | $59 |
| Phase Detector | IH | @ $4 | 1 | @ $4 |
| MP 8616-AO | 8 wks | $429 | 1 | $429 |
| SBC 80/10(A) | 10 wks | $495 | 1 | $495 |
| SBC-064 | 10 wks | $2,200 | 2 | $4,400 |
| SBC-604 | 4 wks | $195 | 1 | $195 |
| Power Supply | 12 wks | $540 | 1 | $540 |
| TOTALS | - | - | 28 | $6,613 |

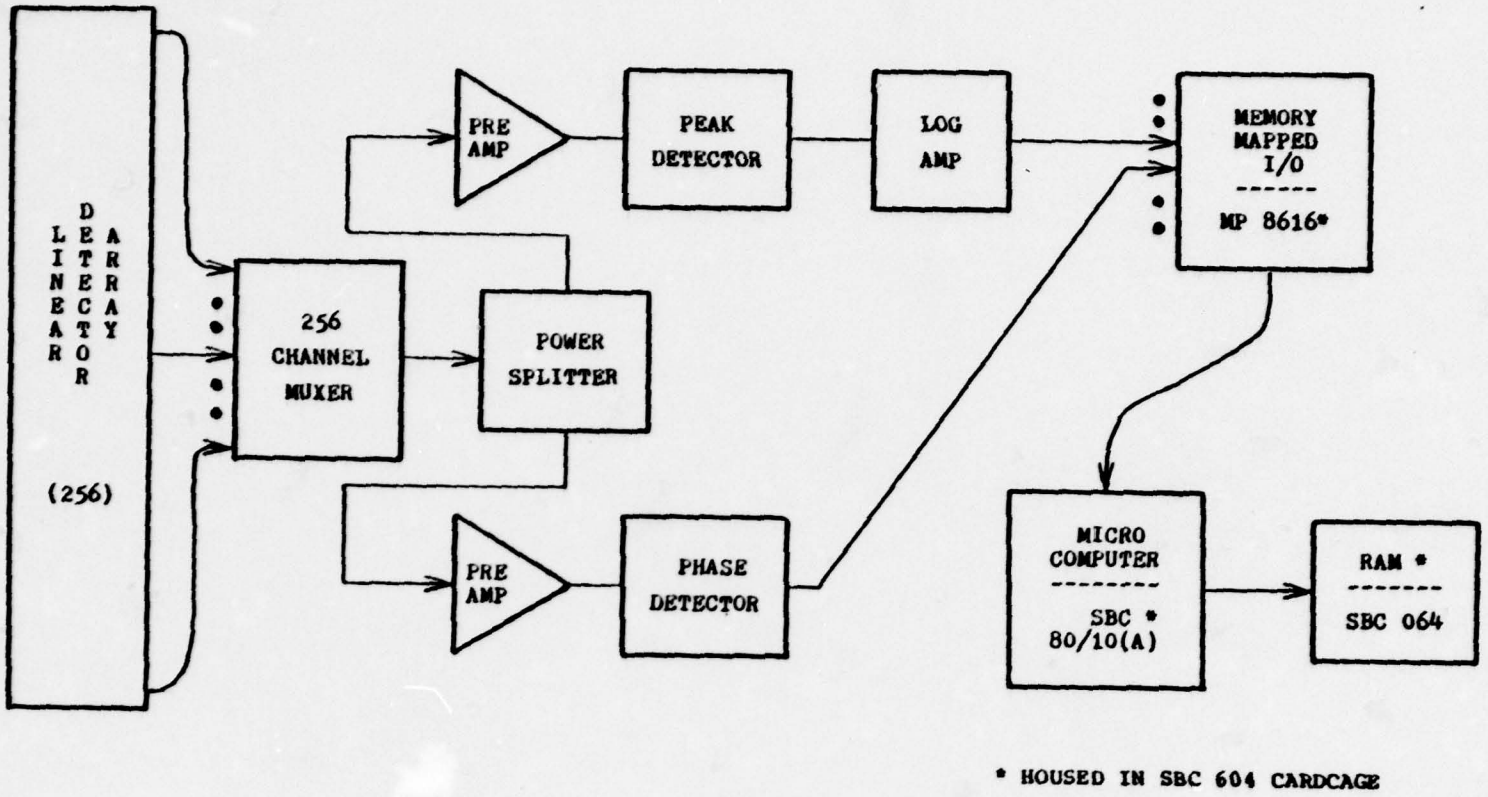



FIGURE 3 - MULTIPLEXED SINGLE CHANNEL DETECTOR SCHEME

C. RECOMMENDATION

The totals tallied literally left no decision as to which scheme was recommended and approved. A further recommendation to pursue work on the multiplexed single channel scheme but with a linear array of 128 detectors, vice 256, was made for the following reasons: (1) to reduce the requirement for two RAM expansion printed circuit boards to one, thereby reducing cost $2,200, (2) to reduce considerably the software and hardware modifications necessary to enable the SBC 80/10(A) microcomputer to access sufficient memory to handle the data generated by a 256 detector scheme, and (3) to build and test a smaller scale prototype before launching into a full scale effort that may not prove feasible in the end. The recommendation was approved.

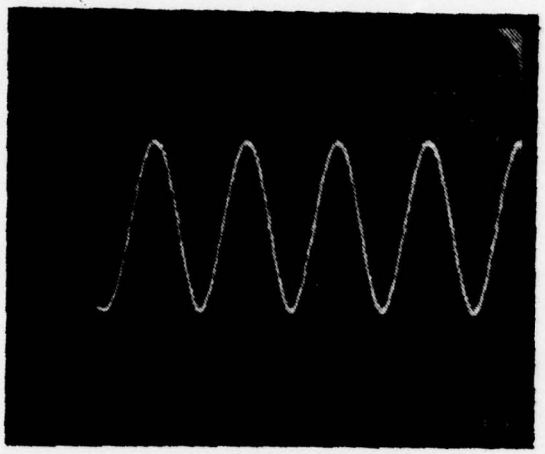
Section VII presents a hardware modification scheme for expanding the memory address capability of the SBC 80/10 (A). Although it has not been tested, it was prepared after close scrutiny of the timing diagrams and handshaking signals required by the CPU of the SBC 80/10(A) and the RAM expansion board.

## III. ANALOG MULTIPLEXER

### A. BASIC COMPONENT

The basic component of the analog multiplexer is the DG 506 complementary MOS (CMOS) 16 channel analog switch. The four bit decoder and device enable logic for channel selection is contained on the integrated circuit (IC) chip. The inputs for such logic are transistor-transistor logic (TTL) compatible. Each channel consists of a pair of CMOS field effect transistors; which in the "ON" condition will conduct current in either direction, and in the "OFF" position will block voltages up to 30 volts peak to peak. The two most critical parameters of this chip are the transition time for a channel to turn ON and the off-channel isolation. Each will be discussed in following paragraphs.

Recall from the introduction the sample time, $T_s$, has now been reduced to 2 ms. As each point in the square matrix is sampled, the gated open detector will allow approximately 2000 cycles of the sinusoidal signal to pass through the multiplexer's "ON" channel to the power splitter. Specifications for the analog switch list the channel on transition time as 0.6 μs. This should distort only the first and last cycles passed during $T_s$ and leave slightly less than 2000 cycles for the amplitude and phase detector channels to execute their functions. Figure 4a shows the first several cycles through the open gate. The



(a) SINGLE CHANNEL ON

Horizontal Scale:
0.5 μs/div

Vertical Scale:
0.5 V/div

(b) ADJACENT CHANNEL TRANSITION

Horizontal Scale:
1 μs/div

Vertical Scale:
0.5 V/div

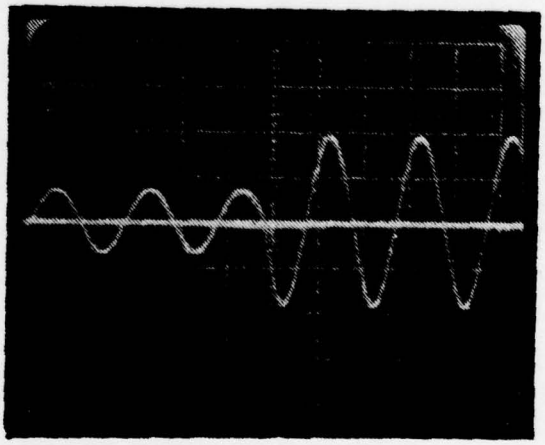


FIGURE 4 - CHANNEL ON TRANSITION TIME

logic that selects this channel is used to trigger an oscilloscope. The triggering edge has been set to occur at the 2nd division line. One can see that approximately one tenth of the first cycle is all that is distorted, which translates to a channel on transition time of 0.1 μs, far exceeding specifications. Figure 4b shows the transition between two sample periods with each signal passed different in amplitude and slightly different in phase. In this application, transition time can be considered "instantaneous."

Off channel isolation refers to a channel's ability to pass the true amplitude and phase of a signal irrespective of adjacent channel signal strengths. Several tests were run to determine the suitability of the analog switch with regard to this parameter.

Characteristic graphs describing this component show off channel isolation as a function of frequency and load resistance. Since frequency is constant in this application, load resistance is the only variable element. For a load resistance, $R_L$, of 1K ohms, off channel isolation is given as greater than 60 dB. Test 1 was run using an $R_L$ of 1K ohms. Four signals of different strengths were applied to four groups of four channels each of a single analog switch. The on-channel attenuation and phase distortion were measured using the Hewlett Packard 3575A Gain-Phase Meter. The upper half of Table III tabulates

| Channel Group | Signal Strength | Input to Channels | On-channel Attenuation | On-channel $\phi$ distortion |
|---|---|---|---|---|
| 1 | -2.9 dBV | 1, 5, 9, 13 | -1.9 dB | -8.8° |
| 2 | -13.8 dBV | 2, 6, 10, 14 | -1.9 dB | -10.6° |
| 3 | -22.8 dBV | 3, 7, 11, 15 | -1.9 dB | -7.2° |
| 4 | -41.8 dBV | 4, 8, 12, 16 | -2.2 dB | -9.4° |

| Constant Channel Group | Channel Group Varied | Output Signal Strength | Constant Channel Group | Channel Group Varied | Output Signal Strength |
|---|---|---|---|---|---|
| 1 | 2 | -4.9 dBV | 3 | 1 | -24.9 dBV |
| | 3 | -4.8 dBV | | 2 | -24.7 dBV |
| | 4 | -4.8 dBV | | 4 | -24.8 dBV |
| 2 | 1 | -15.8 dBV | 4 | 1 | -44.0 dBV |
| | 3 | -15.7 dBV | | 2 | -43.9 dBV |
| | 4 | -15.7 dBV | | 3 | -43.9 dBV |

TABLE III. Test 1 Data on Analog Switch

this data. One channel of a group was addressed and the signal to that channel held constant while signals to the other three channel groups were varied over a range of -60 dBV to 0 dBV. (All power levels hereafter expressed in terms of dBV are rms values.) The signal strength of the constant channel at the switch output was measured and tabulated in the lower half of Table III. In each case the output signal strengths reflected only the on-channel attenuation measured earlier and none of the varying signal strengths on adjacent channels.

Not reflected in Table III but noted during Test 1, output signal phase distortion did not remain constant when adjacent channel signals were varied. In particular the weaker signals through channel groups 3 and 4 experienced as much as 5° additional phase distortion beyond their characteristic on-channel phase distortion measured earlier. Test 2 was run to select a load resistance that would reduce this fluctuation.

In this test a constant signal strength was applied to an ON channel of the switch. On channel attentuation and phase distortion were then measured as $R_L$ was varied. Results are tabulated in Table IV.

Data taken by previous students using the original system indicated that amplitude variation from channel to channel did not fluctuate greatly. In many instances, however, phase variation did fluctuate greatly and thus was considered the more sensitive of the two parameters.

Therefore an $R_L$ of 100Ω was selected because it perturbed the phase the least as a signal passed through the analog switch. Even though on-channel attenuation was greatest with this choice, signal strength could be amplified as necessary in the amplitude detector channel for accurate results. Switch specifications showed that off channel isolation improved as the load resistance decreased, therefore I did not consider it necessary to rerun Test 1 using an $R_L$ of 100Ω. Now satisfied with the performance of the basic component, I commenced to design the multiplexer.

| $R_L$ (Ω) | On-channel attenuation | Phase distortion |
|---|---|---|
| 100 | -10.3 dB | -0.3° |
| 200 | - 6.8 dB | -2.5° |
| 300 | - 4.9 dB | -3.8° |
| 560 | - 3.0 dB | -5.0° |
| 750 | - 2.4 dB | -5.4° |
| 1K | - 1.9 dB | -5.8° |
| 2K | - 1.0 dB | -6.5° |
| 3K | - 0.6 dB | -6.8° |
| 3.9K | - 0.2 dB | -7.2° |

TABLE IV. Test 2 Data on Analog Switch

B. CHANNEL SELECTION LOGIC

The multiplexer was designed for eventual use with the 256 linear detector array. Actual construction and testing of the 128 channel system was done using half the multiplexer's channel capacity. Sixteen of these analog switches were aligned in parallel to accommodate the 256 outputs from the linear detector array. The outputs of these sixteen were buffered and fed into a seventeenth switch creating a 256 channel 2 level analog multiplexer. Buffering was necessary between the two levels because of an impedance mismatch. The load resistance on first level outputs was 100Ω. The input impedance measured at the second level was 50Ω. Buffering was accomplished using a high speed unity gain voltage follower operational amplifier, LM 310, wired as shown in Figure 5.

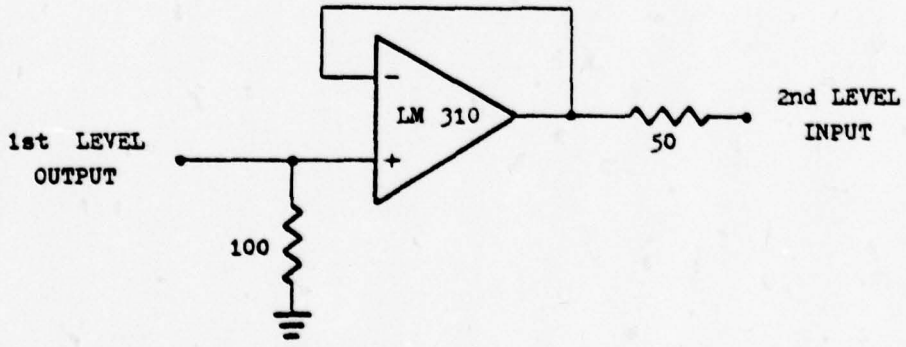



FIGURE 5 - MULTIPLEXER BUFFER

The upper four bits of an 8 bit counter were input to a one of sixteen decoder. The decoder outputs enabled each of the first level switches sequentially. Since the decoder outputs are active low and the chip enable for the DG 506 is active high, it was necessary to invert the decoder outputs. As each of the sixteen switches was enabled, the lower four bits of the 8 bit counter selected each of the sixteen channels sequentially. The second level switch was permanently enabled. Channel selection in this switch is accomplished with the upper four bits of the 8 bit counter. Figure 6 presents a block diagram of the channel selection logic.

C. CLOCK LOGIC

The sample period has already been determined to be 2 ms. Therefore a clock was needed that put out a TTL compatible square wave pulse at 500 Hz. Figure 7 shows a simple RC inverter circuit that generates a rectangular pulse of variable period. Looking at the output on an oscilloscope, it was noted that the duty cycle was not 50% and the waveform was quite noisy. To clean this up, the signal frequency was adjusted to 1000 Hz and fed to the clock input of a J-K flip-flop wired as a toggle flip-flop. This divided the frequency by two and resulted in a very clean square wave output. The two counters advanced on the falling edge of the clock input.

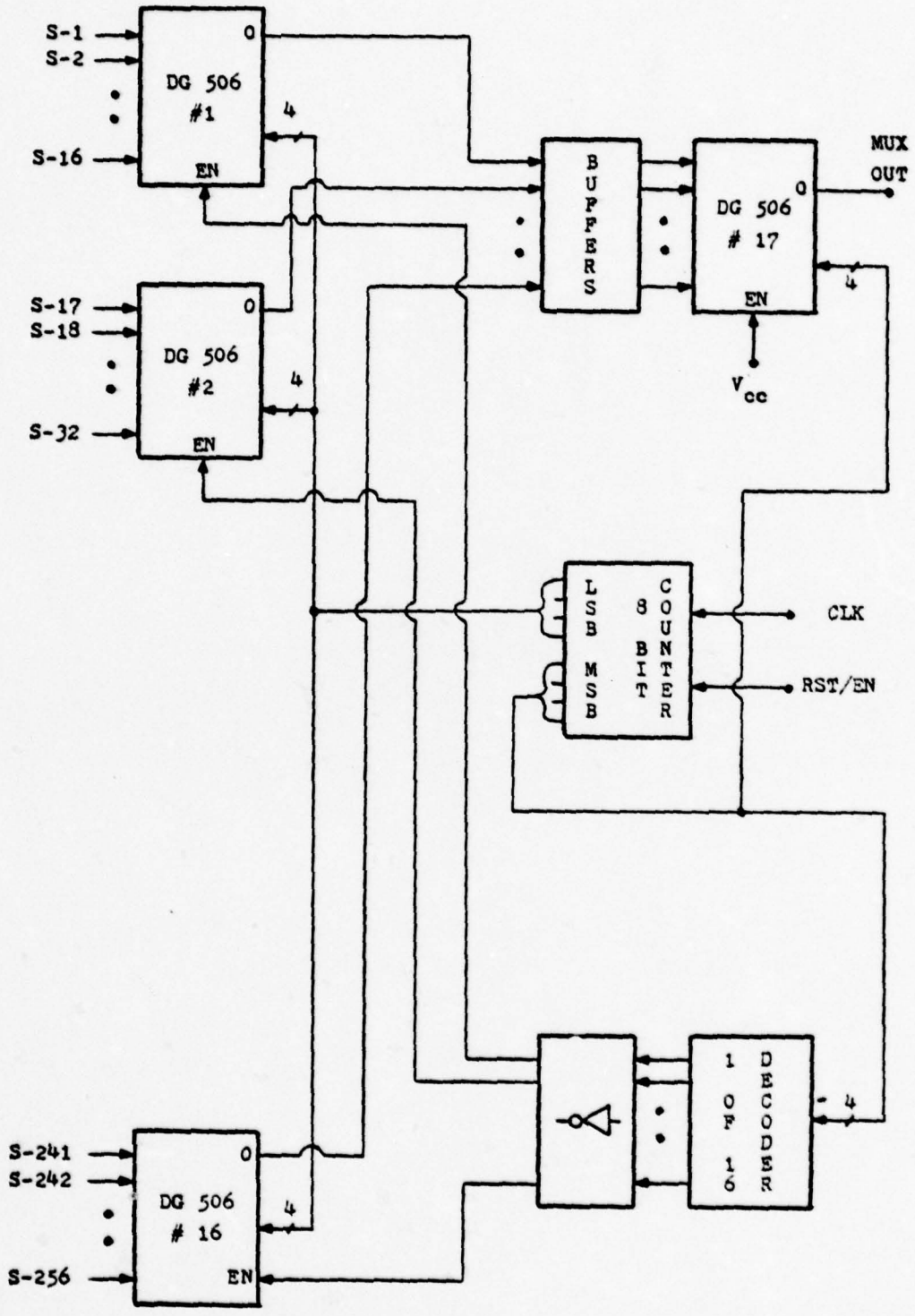



FIGURE 6 - CHANNEL SELECTION LOGIC FOR 256 CHANNEL 2 LEVEL MULTIPLEXER

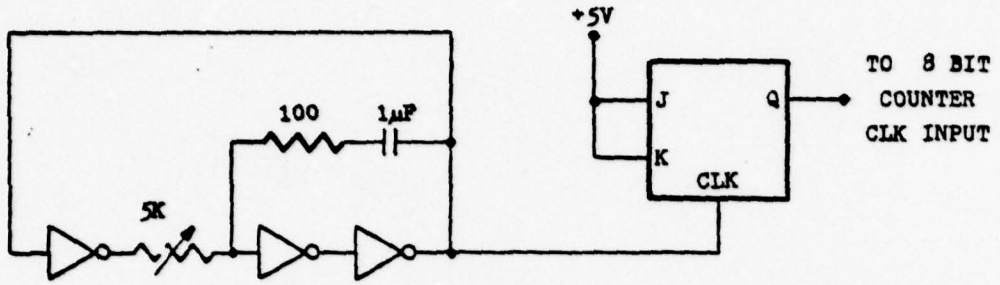



FIGURE 7 - MULTIPLEXER CLOCK LOGIC

D. ENABLE/RESET LOGIC

There exists on the original system circuitry that counts samples as they are taken (every half second) during each horizontal scan of the ultrasonic probe. The signal generated with each sample that goes to the counter also lights up a light emitting diode (LED). Recall that a design objective of this thesis was to take an entire column of samples in the time one sample was taken with the original system. Hereafter, the above LED is referred to as the "sample column LED."

For the 8-bit counter in the channel selection logic, two 7493 4-bit binary counters were cascaded. These IC chips each have two reset inputs. Both must be high in order to reset the counters. The counters will remain stagnant until either one or both inputs is dropped low. In this application one reset input has been permanently wired high on each counter. The other input is controlled by the output of a J-K flip-flop.

The J and K inputs, which come from the microcomputer of the data processing unit, are normally held low. A high on the J line will set the flip-flop and thereby reset the counters. They will remain reset until a high on the K line is sent. This will reset the flip-flop and consequently enable the counters. Software of the microcomputer is such that a high signal is never sent simultaneously to both the J and K inputs.

In an effort to streamline the design of the clock and enable/reset logic, a dual J-K flip-flop IC chip was used. The clock frequency applied to one half of the chip was 1 KHz. The clock frequency for the enable/reset flip-flop, which also came from the microcomputer, was 9.21 MHz. When the data processing unit was completed and connected to the multiplexer for testing, debug operations led to the conclusion that when two flip-flops on the same IC chip are clocked at widely separated frequencies, one will have a definite, but unpredictable, effect on the other. Using flip-flops on two separate IC chips solved this problem. Also the liberal use of despiking capacitors helped to prevent further interaction within and amongst IC chips in other circuits.

## E. DYNAMIC RANGE TESTS

All tests to this point were conducted on individual components. Testing of the 128 channel multiplexer as a complete unit now proceeded, with particular regard to its input dynamic range.

To check this a sinusoidal signal was input to selected channels and its strength varied over a range from -50 dBV to +10 dBV. Several channels from three of the eight internal switches were tested. The on-channel attenuation and phase distortion was measured through each. All channels but the ON channel were grounded because of another hard learned lesson. It was found that if all channels but the ON channel were not grounded, the wires leading to the other fifteen channels picked up stray electromagnetic radiation in the air, which adversely affected the data taken with each test measurement. If a range could be found over which the amplitude attenuation and phase distortion were minimum, or if not minimum, at least constant, then a correction factor could be added later in software, either by the microcomputer or the PDP-11/50 computer. Figures 8 and 9 represent the average of all data taken as a function of input signal strength. Amplitude attenuation is relatively constant (within 1 dB) between -40 dBV and +10 dBV, while phase distortion is relatively constant (within 1.5°) only between -35 dBV and +5 dBV. Using the limits in parentheses as criteria, the dynamic range of the 128 channel analog multiplexer was established as 40 dB, with the lower and upper limits at the input at -35 dBV (rms) and +5 dBV (rms) respectively. Amplitude attenuation between these limits rounds off to -10 dB. Another 3 dB is lost when the output is divided between the amplitude and

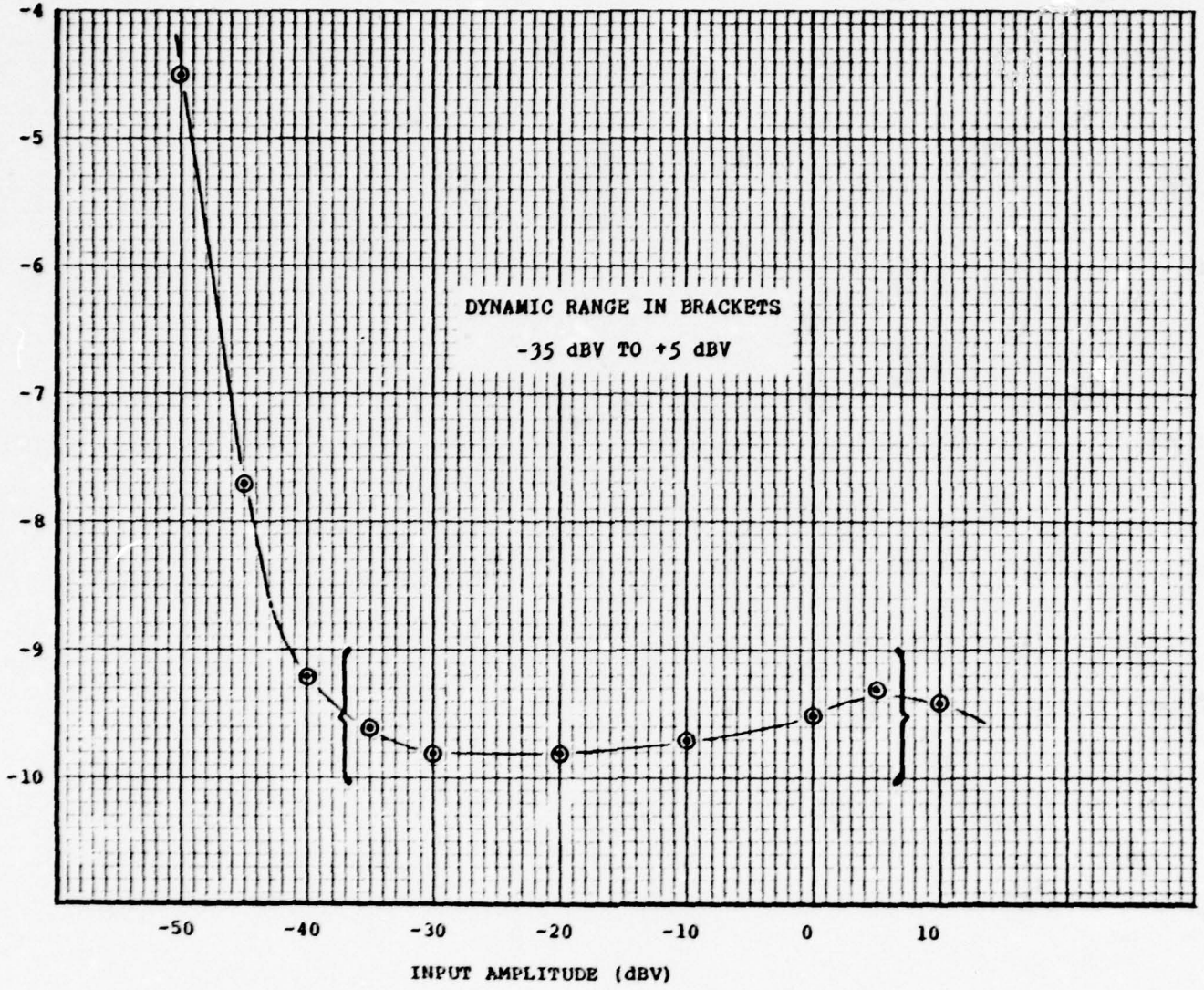



FIGURE 8 - AMPLITUDE ATTENUATION THROUGH MULTIPLEXER

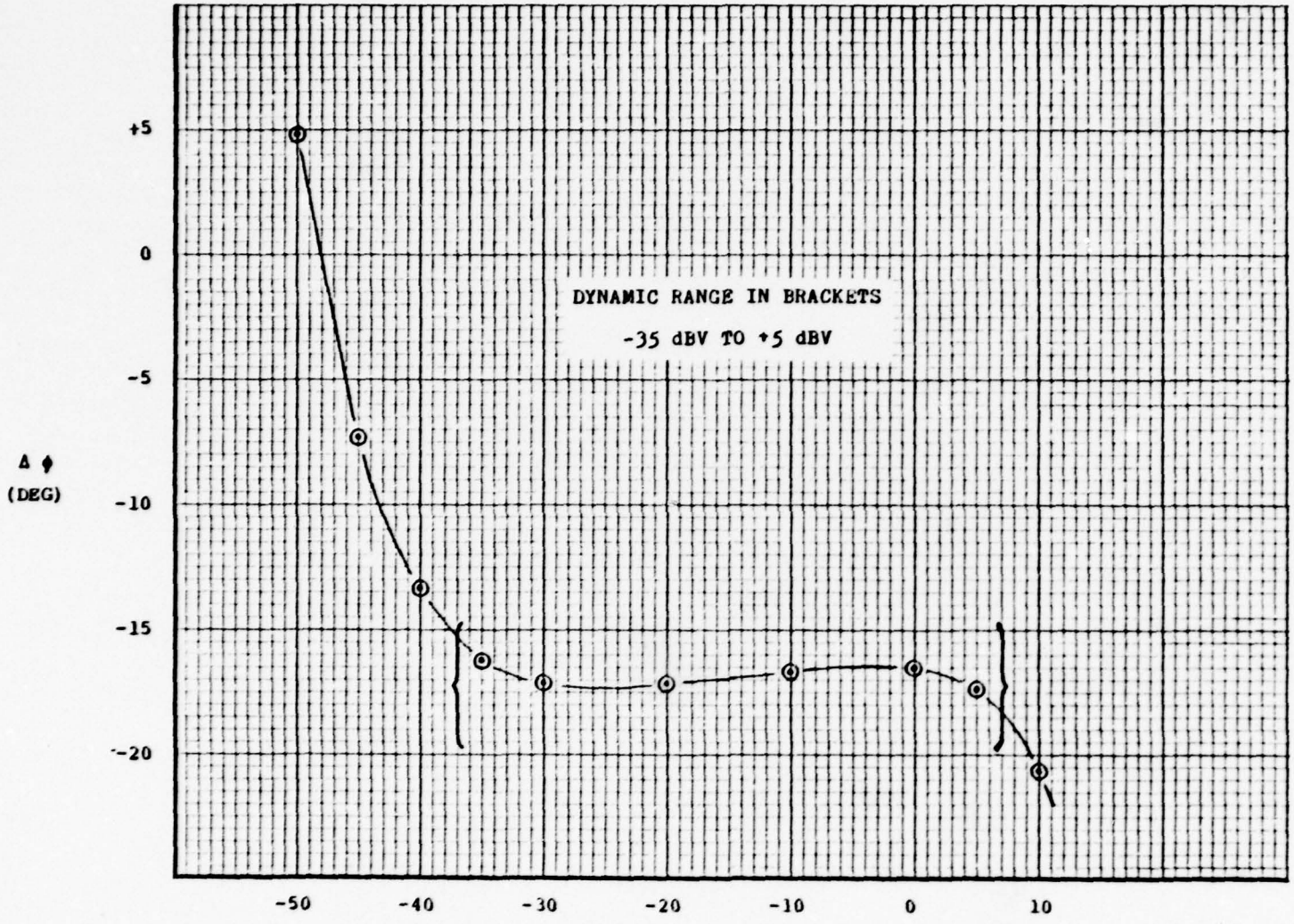



FIGURE 9 - PHASE DISTORTION THROUGH MULTIPLEXER

phase detection channels by the power splitter. Therefore the voltage range seen by each of the detection channels runs from -48 dBV (rms) to -8 dBV (rms).

# IV. PHASE DETECTION

## A. CIRCUIT DESCRIPTION

Given $T_s$ of 2 ms, or approximately 2000 cycles each of the reference and detected signals, a circuit that could measure the phase difference between the two in half that time was desired. The second half of the period could then be used to process and store the results by the data processing unit. Figure 10 shows a diagram of a circuit slightly modified from one found in Ref. 4. Components $A_1$ and $A_2$ are two LM 710 high speed comparators. The back to back diodes at their inverting inputs hard limit the signals and set the lower end of the amplitude range at 0.5 volts. The two comparators square up the clipped inputs. The NAND gates buffer and invert the outputs before being applied to two toggle flip-flops. The additional NAND inverter in the reference channel serves to set a midscale zero-phase difference reading at the circuit output. Two J-K flip-flops wired as toggle flip-flops, similar to the clock flip-flop in the multiplexer, divide the signal frequencies in half, but more importantly, their phase difference also. The four cascaded NAND gates perform an exlusive OR function on the two flip-flop outputs. The output of this composite exclusive OR gate is a train of width modulated pulses, the duty cycle of which is proportional to the phase difference between the two

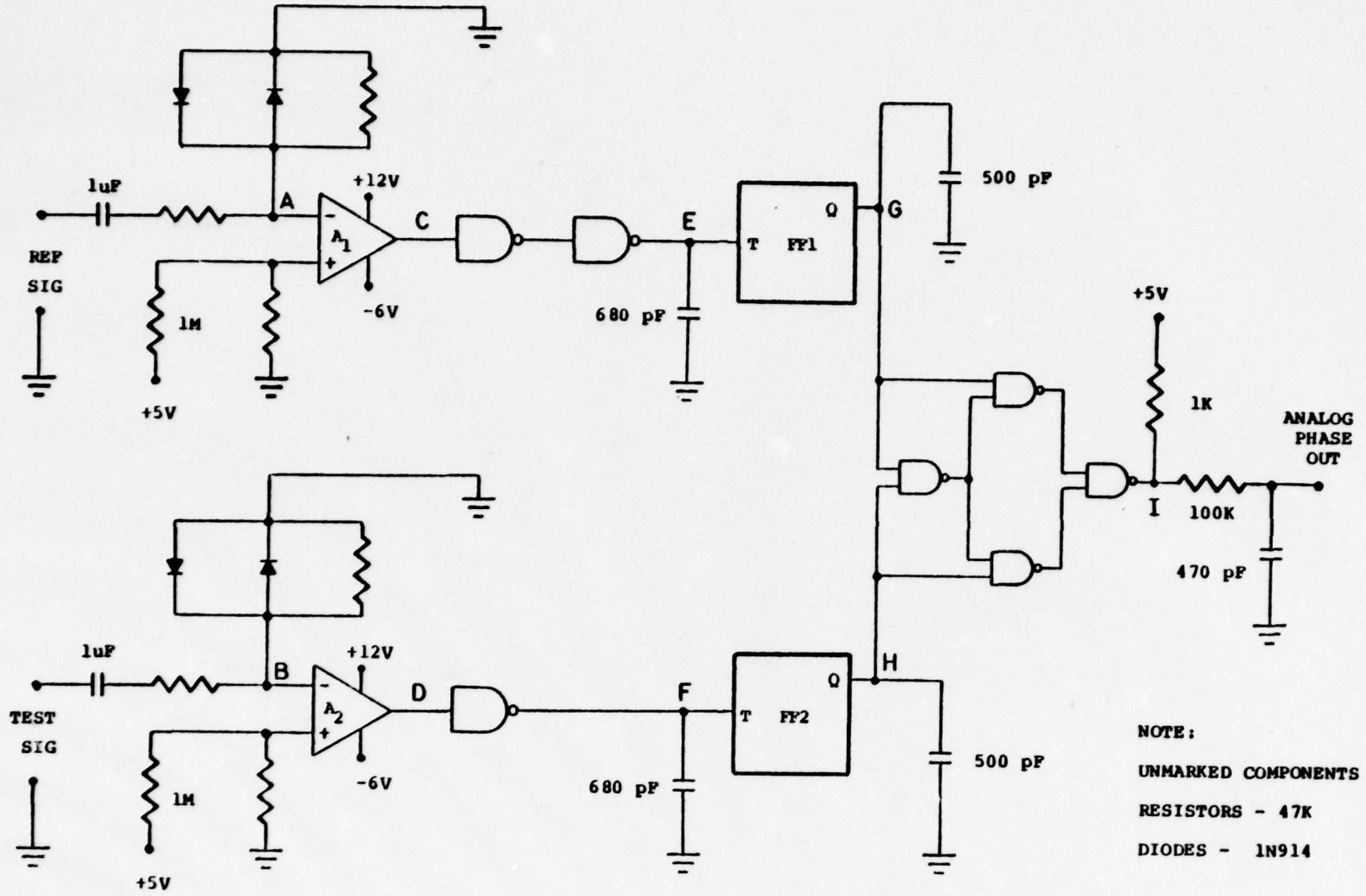



FIGURE 10 - PHASE DETECTOR CIRCUIT

input signals. The pullup resistor at the output and the biasing of the NAND gates set the output range from 0 to 5 volts. This pulse train is applied to a fast integrator which yields an analog voltage proportional to the phase difference.

The exclusive OR operation by itself would only be able to detect a ±90° phase difference relative to the reference. Due to the toggle flip-flops, the ±90° limit equates to ±180° and thus enables phase difference measurements over the full range of 360°. When testing the circuit at several points with a probe from an oscilloscope, overshoots and ringing at transition times of the square waveforms were observed. Despiking capacitors placed at these points smoothed out the transitions nicely. Figure 11 shows the waveforms observed at lettered points in the circuit. Two in-phase signals were chosen to illustrate how the additional NAND buffer/inverter in the reference channel sets a zero-phase midscale reading. The flip-flops toggle on the falling edges of their clock inputs. Note Waveform I has a 50% duty cycle which, when applied to the integrator, will yield an output of 2.5 volts.

## B. CIRCUIT TESTING

Two circuit tests were run to ascertain the phase detector's suitability for the system under design. Test 1 was run to determine the transfer characteristic of the circuit. Test 2 determined the time response of the circuit.

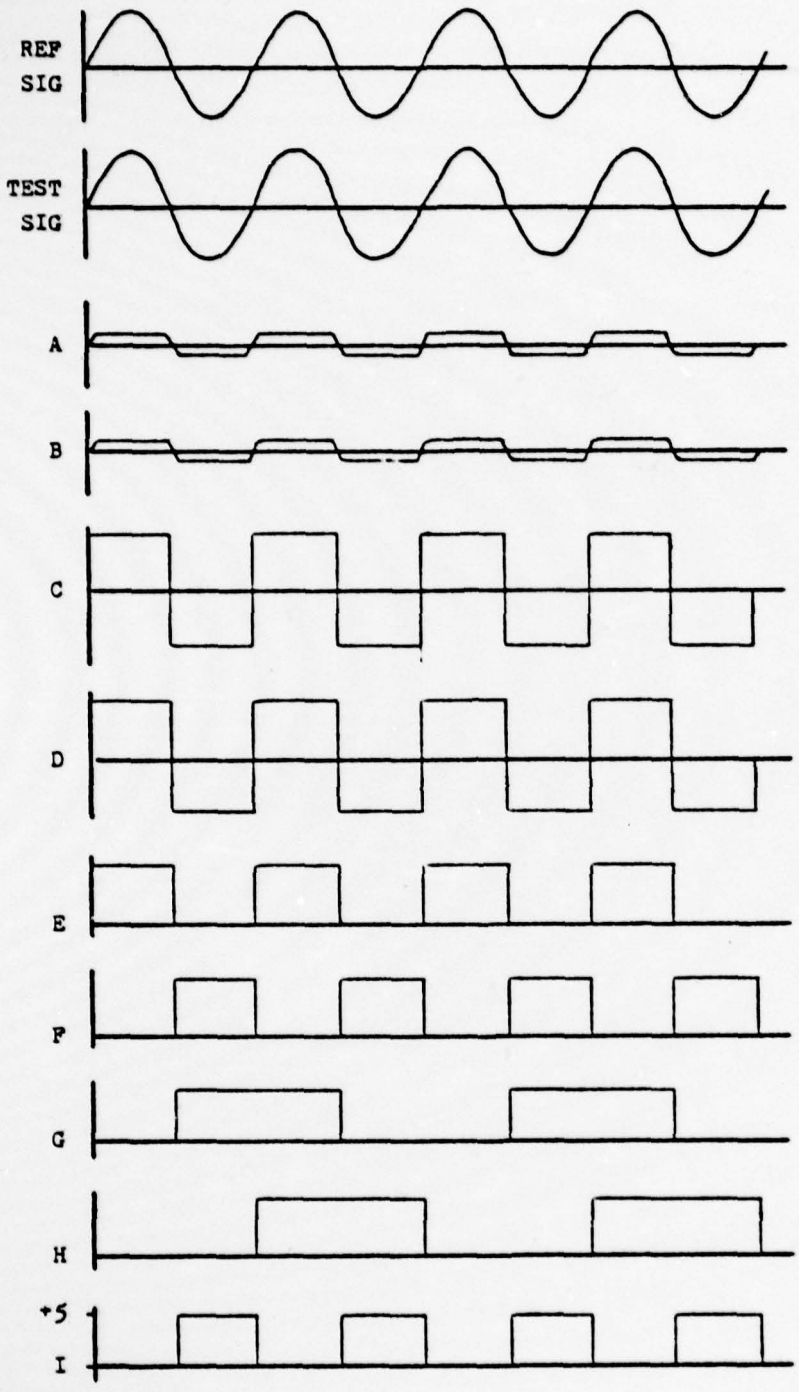



FIGURE 11 - TIMING DIAGRAM FOR PHASE DETECTOR CIRCUIT

In Test 1 continuous signals of approximately equal amplitude were applied to the detector circuit and the phase of one varied ±180° relative to the other. Several runs were made at different amplitude levels. The results of two runs are shown in Figure 12. The best, or most linear, results were obtained when the input amplitudes were greater than or equal to 15 dBV. This would require the detected signal from the multiplexer, ranging from -48 dBV to -8 dBV, to be amplified, in the worst case, by 63 dB. Additionally, amplification would have to be non-linear in nature because boosting a -8 dBV signal by 60 dB would produce a signal that would blow out the detector circuit. This problem is addressed in the next section.

To test the time response of the circuit two in-phase signals were applied to the same respective channel on two analog switches. The outputs of the two switches were applied to the inputs of the phase detector. The channels on the two switches were gated open simultaneously by a common counter for 1.7 ms. One of the switch outputs was applied to the upper channel of a dual trace oscilloscope. The output of the phase detector was applied to the lower channel. The oscilloscope was set to trigger on the upper trace. Figure 13 shows the time response of the phase detector circuit. The upper trace is blurred because it includes approximately 1700 cycles of the signal. The lower trace is blurred because the intensity had to be

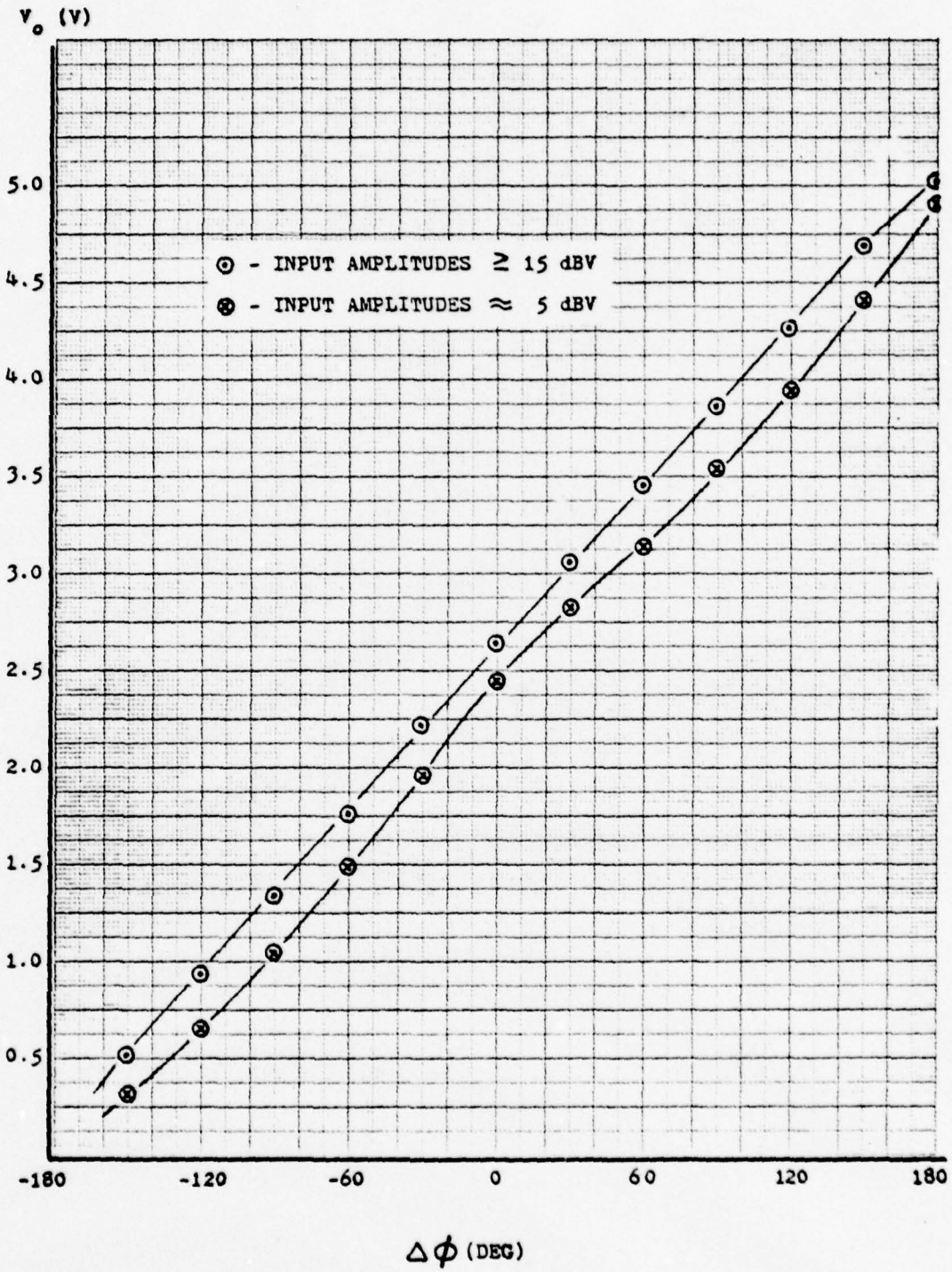
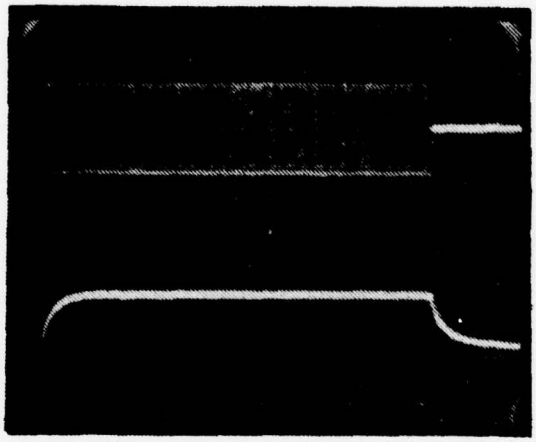



FIGURE 12 - PHASE DETECTOR TRANSFER CHARACTERISTIC

turned way up in order to see the faint upper trace. Recall that 1 ms is allowed for this circuit to perform its function. The figure clearly shows that steady state output is reached in about 0.2 ms. From the vertical scale, one can see the output rests at about 2.5 volts,



Horizontal Scale: 0.2 ms/div  Vertical Scale: 2 V/div

FIGURE 13 - PHASE DETECTOR TIME RESPONSE

which equates to a zero-phase difference between the two input signals.

C. PREAMPLIFICATION

To provide the worst case necessary preamplification, two ANZAC AM-110 wideband 30 dB amplifiers were cascaded. Biasing the amplifiers with 20 volts and ground theoretically limits their output to a maximum of 10 volts peak or 17 dBV.

Experimental measurements showed that once input amplitudes exceeded -40 dBV, the average output strength leveled at 20.3 dBV, with the maximum climbing at one point at 22.1 dBV. Also at the lower amplitude levels, -50 dBV to -45 dBV, as much as 64.2 dB of gain was realized. So the amplifiers functioned a little better than advertised. The upper bound had the effect of limiting amplification of signals greater than -40 dBV and thus produced the nonlinear effect needed. Phase distortion passing through these amplifiers turned out to be amplitude dependent.

The power splitter remained the only component left where possible phase distortion could be measured. Distortions here turned out to be amplitude independent and relatively constant at about -1.9°. Table V tabulates data taken when testing both the ANZAC AM-110 amplifiers and the power splitter. Figure 14 plots this data. Both these phase distortion error sources constitute correction factors that must be accounted for before final processing by the PDP 11/50 computer.

| | 2 ANZAC Amplifiers | | | Power Splitter |
|---|---|---|---|---|
| IN(dBV) | Out(dBV) | Amp(dB) | $\Delta\phi(°)$ | $\Delta\phi(°)$ |
| -50 | 14.2 | 64.2 | +31.5 | -2.1 |
| -45 | 18.4 | 63.4 | 28.7 | - |
| -40 | 20.4 | 60.4 | 22.9 | -2.3 |
| -35 | 21.0 | 56.0 | 16.6 | - |
| -30 | 21.5 | 51.5 | 11.8 | -2.0 |
| -25 | 22.1 | 47.1 | 8.0 | - |
| -20 | 21.5 | 41.5 | 3.7 | -1.6 |
| -15 | 18.5 | 33.5 | -1.0 | - |
| -10 | 17.9 | 27.9 | -4.5 | -1.5 |
| -5 | 19.1 | 24.1 | -6.8 | - |
| 0 | 20.4 | 20.4 | -8.5 | -1.4 |

TABLE V. Phase Distortion in Preamplifiers and Power Splitter

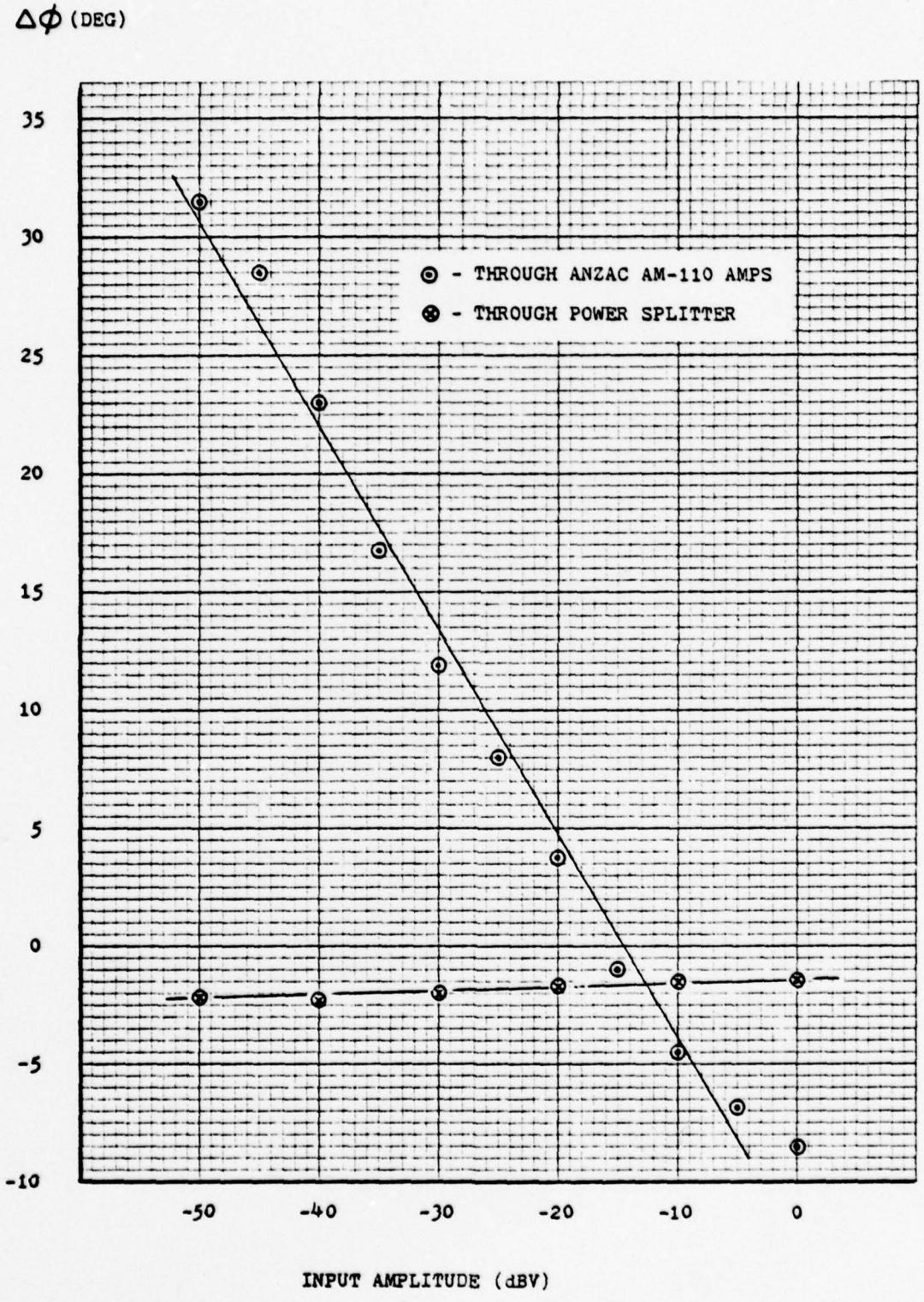



FIGURE 14 - PHASE DETECTOR PREAMP CHARACTERISTICS

# V. AMPLITUDE DETECTION

## A. PEAK DETECTOR

The component chosen for the present system was the Model 5006 Peak-to-Peak Detector from Optical Electronics Incorporated. Its input voltage range runs from 30 mV to 10 V peak, or -33.5 dBV to 17 dBV. Its output is a dc voltage over the same range. Its frequency response is rated at being able to measure the peak amplitude (within a 2% error) of a single cycle of input for up to 3 MHz sinusoidal signals. As with the phase detector, the first half of $T_s$ is dedicated to measuring the amplitude. Having 1000 cycles of a 1 MHz signal reduces this 2% error even further and allows steady state output to be reached almost instantaneously. Contributing to this virtually instant steady state response is an output decay rate of 0.5 V/μs. When the multiplexer transitions from channel to channel, the detector can change its output to measure the new amplitude in a matter of several microseconds. According to specifications the device is tailor made for the amplitude detection channel under design.

## B. LOGARITHMIC AMPLIFIER

Given an input dynamic range from -33.5 dBV to 17 dBV, it was necessary to logarithmically amplify this range to within a 10 volt range from -5V to 5V to be compatible with the analog input peripheral board of the data processing

unit. The Model 755N Log Amplifier made by Analog Devices has this capability. Its input voltage range runs from 1 mV to 10V peak. This makes it easily compatible with the peak detector's output range. Frequency response is of no concern since its input is a slowly varying dc voltage. Rise time for the voltage levels of concern is between 4 μs to 7 μs. Allowing three time constants for the output to settle, steady state output can be reached in approximately 20 μs, well within the 1 ms allowed for amplitude detection. The transfer function for the log amplifier is

$$E_o = -K \log \frac{E_{sig}}{E_{ref}} \quad ,$$

where K is a user selectable gain, $E_{sig}$ is the dc voltage output of the peak detector, and $E_{ref}$ is a reference voltage internally set at 0.1 volts.

## C. CIRCUIT TESTING

The circuit diagram is relatively simple and is shown in Figure 15. To verify the transfer function of the entire circuit, a 1 MHz test signal was applied to the input and varied over the input range of the peak detector. The transfer characteristic is plotted in Figure 16. The straight line shows the transfer characteristic according to specification. The plotted points indicate actual measurements after adjusting the trim pot resistors on each component. Measurements tracked specifications

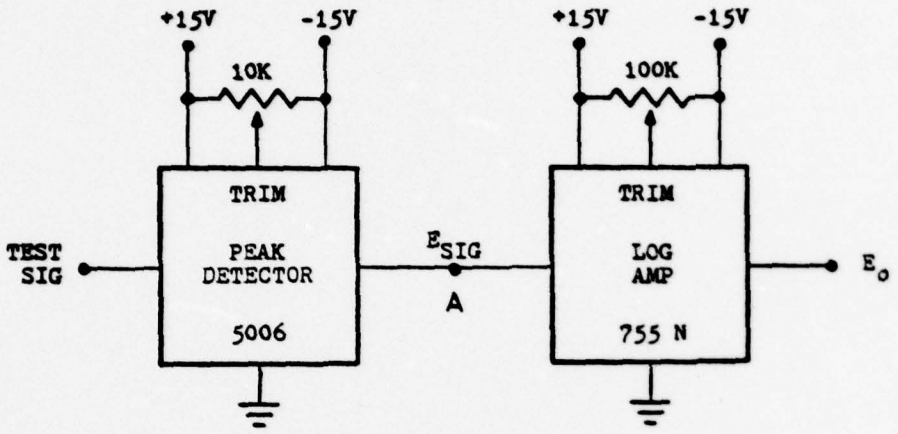



FIGURE 15 - AMPLITUDE DETECTOR CIRCUIT

pretty closely for the higher input voltages. At the low end appreciable differences were observed. The next step was to check for possible impedance mismatch between components. The peak detector has an input impedance of 1000 ohms and requires a like load impedance. The input impedance of the log amplifier was measured at 10 ohms. Using an LM 310 buffer at point A in Figure 15, the two dissimilar impedances were matched in a manner similar to the method described in Figure 5, Section III for the analog multiplexer. When testing continued at this point the peak detector module malfunctioned. A replacement component could not be obtained in time to complete testing and present the results in this thesis.

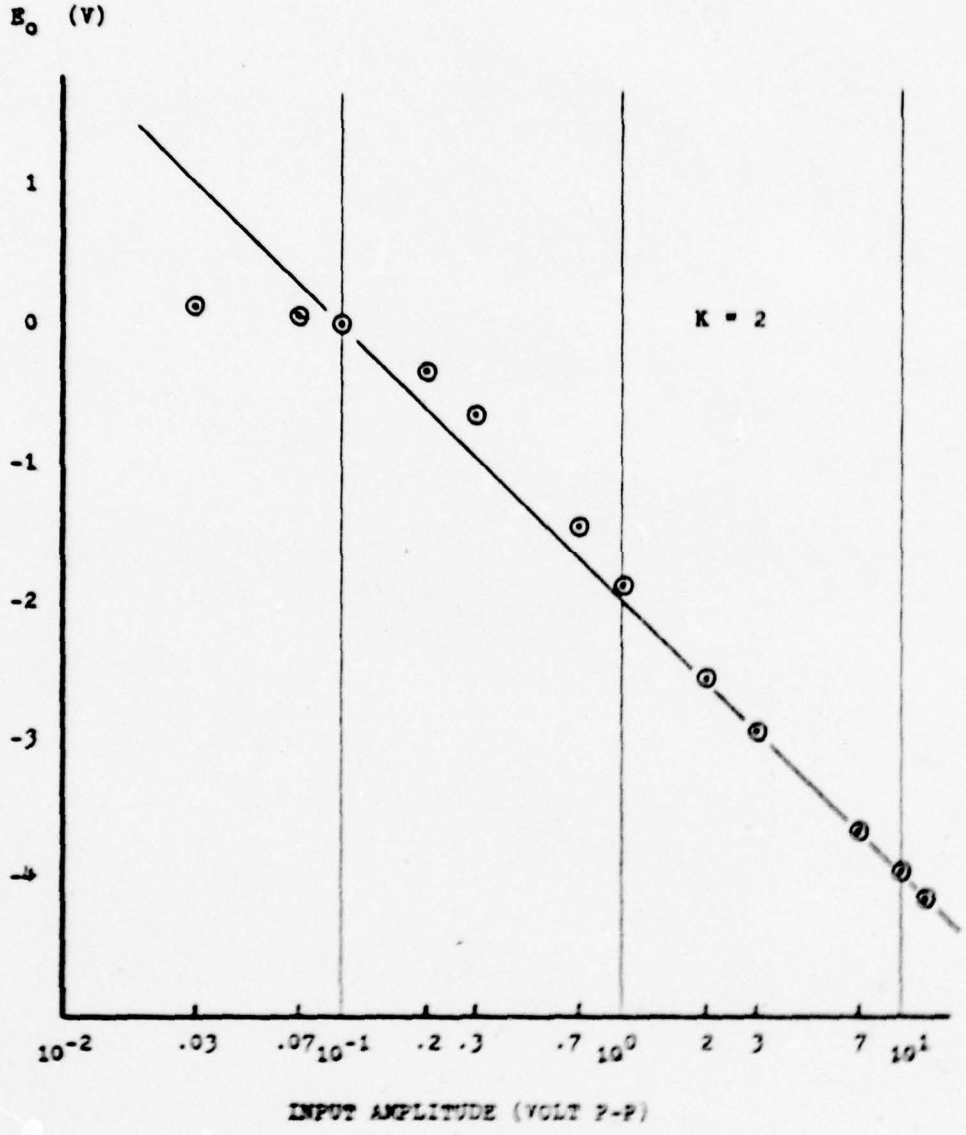



FIGURE 16 - AMPLITUDE DETECTOR TRANSFER CHARACTERISTIC

Although actual measurements diverged from specifications in the lower input voltage range, there did exist a 40 dB range, or two voltage decades, over which performance did fairly closely match specifications. It is the author's opinion that with proper impedance matching between the test signal source, hardware components, measurement equipment and some more fine trimming of the variable resistors, this circuit will yield results much more closely resembling specifications.

## D. PREAMPLIFICATION

The dynamic range of the data acquisition system thus far has been set by the range of the analog multiplexer, -48 dBV to -8 dBV at its output. The range over which test results on the amplitude detector were most linear ran from 0.1 V to 10 V, or -23 dBV to 17 dBV. To make the output range of the multiplexer compatible with the input range of the amplitude detector, 25 dB of amplification is needed. With components on hand, an ANZAC AM-110 wide band 30 dB amplifier in series with an attenuator will provide the necessary amplification.

## VI. DATA PROCESSING UNIT

### A. MAJOR COMPONENTS

#### 1. SBC 80/10(A)

The heart of the data processing unit (DPU) is the SBC (Single Board Computer) 80/10(A) from Intel. A general description follows here; more detailed descriptions follow in sections that discuss specific operations that exploit the numerous capabilities of the SBC 80/10(A). The system is a complete microcomputer on one 6.75 x 12 inch printed circuit board. It has the 8080A CPU, system clock, random access memory (RAM), non-volatile read only memory (ROM), parallel and serial input/output capability and bus control logic. The 8080A CPU is an 8-bit n-channel MOS (NMOS) IC chip with an accumulator and six general purpose registers, all of which are used in software programs to follow. It has a stack pointer register which establishes a last in/first out (LIFO) stack anywhere in RAM, and a 16-bit program counter which will address up to 64K bytes of memory. 1K bytes of RAM reside on the board along with sockets for up to 8K bytes of ROM. The system clock operates at 2 MHz, but another clock at 9.21 MHz exists for user needs.

#### 2. MP 8616-AO Analog Input/Output Board

Data presented to the DPU from the amplitude and phase detection channels is in analog form. It must be converted to digital form before the 8080A CPU can process

it. This is accomplished with the MP 8616-AO Analog Input/ Output (I/O) Board from Burr-Brown. This peripheral board was designed specifically to be compatible with several of Intel's microcomputer systems, one of which is the SBC 80/10(A). The input voltage range is user selectable; in this case plus/minus five volts is used to accommodate the output ranges of the two detection channels. The board has 16 memory mapped analog input channels. An analog multiplexer will select any of these channels by decoding the memory address associated with a channel. Memory assignments are also user selectable by means of on board jumper connections. Once selected an analog signal is amplified and routed through an 8-bit A/D converter to a data bus interface. Control and timing logic on board will receive and generate the handshaking signals necessary to transfer data to the CPU. To access analog data, one need merely execute a standard 8080A memory read instruction, using as an address one of the memory locations assigned to the analog I/O board. This command initiates A/D conversion which takes 44 μs. A second like command will transfer the now converted digital data over a common data bus to the accumulator of the CPU.

3. SBC-064 RAM Expansion Board

A 128 square sample matrix equates to 16K samples. At two data bytes (amplitude and phase) per sample, 32K bytes of data will be generated in this operation. With

only 1K of on board RAM, considerable additional memory is needed. The SBC-064 from Intel provides an additional 64K byte capacity of RAM. For the 128 detector scheme only half this capacity is needed, but for the eventual 256 detector scheme, 128K bytes of data storage will be needed. Hence the need for a second RAM board referred to in Section II. The SBC-064 is electrically and mechanically compatible with the SBC 80/10(A).

4. SBC 604 Cardcage and MULTIBUS

The three previous boards can be interfaced via a common MULTIBUS, an Intel trademark. The 86 line MULTIBUS consists of a 20 line address bus, 16 line bidirectional data bus, a control bus over which handshaking and timing signals are exchanged, several interrupt lines, and power supply lines. Of the three modules using the MULTIBUS, the SBC 80/10(A) is the bus master, and the other two are bus slaves. Multiple master modules may share the MULTIBUS, but then there is a need for bus arbitration. Several control bus lines are devoted to this task. In this system, since there is only one master, these lines go unused. On all three modules these 86 lines terminate on an edge port P1. The SBC 604 Cardcage houses up to four 6.75 x 12 inch modules. Each module fits into a slot terminated with an 86 pin edge connector. The four connectors are interconnected by a internal mother board. By seating the P1 ports of the three modules of this system into the edge

connectors of the SBC 604, they are then connected via the common MULTIBUS.

5. SBC 635 Power Supply

Power requirements for the present system are listed in Table VI. Underneath the "Totals" line are listed the amperage and voltage levels provided by the SBC 635 power supply from Intel. This unit was purchased because it not only provides power needed for this system, but also can easily provide the power for the additional SBC-064 needed for a 256 detector scheme. The power supply connectors easily mate to the SBC 604 Cardcage.

| Module | +5V | +12V | -5V | -12V |
|---|---|---|---|---|
| SBC 80/10(A) | 2.9A | 150 mA | 2 mA | 175 mA |
| SBC 064 | 3.2A | 600 mA | 40 mA | - |
| MP 8616-AO | 2.0A | - | - | - |
| Totals | 8.1A | 750 mA | 42 mA | 175 mA |
| SBC 635 | 14.0A | 2.0 A | 900 mA | 800 mA |

TABLE VI. Power Requirements for Data Acquisition Systems

### 6. Integration with Other System Components

To control the operation of the data acquisition system, the DPU must synchronize itself with the timing of other system components. To achieve this it must provide signals to and test other signals from the multiplexer and the original system. DPU outputs include enable, reset and clock pulse signals to the enable/reset J-K flip-flop in the multiplexer. The enable and reset pulses are generated in software. The clock is derived from the 9.21 MHz clock provided by the SBC 80/10(A). DPU inputs include analog amplitude and phase voltages, the multiplexer's clock, sample column LED, and a "Write Start" interrupt signal. These signals pass to and from the DPU through a control panel. The control panel has other switches to (1) generate a "Read Start" interrupt signal, (2) externally reset the entire system, and (3) set the system for operation in the write or read mode. Two indicator LED's complete the panel to let the user know when read or write operations are completed. Within the DPU these signals pass from the control panel to the CPU through the common edge port P1, port J1 and J2 of the SBC 80/10(A), and port P3 of the MP 8616-AO analog board. A detailed listing of all port connections is contained in Appendix E.

## B. SOFTWARE

Software was developed and tested using the Tektronix 8002 Microcomputer Development System in Emulation Mode 1.

Once final debugging was achieved, the software was burned into an 8708 Electrically Programmable ROM (EPROM) and tested again in Emulation Mode 2. The software is broken down into three sequences: (1) a power up sequence, (2) write operation, and (3) read operation. The software program for each sequence is included in Appendix F.

1. Power Up Sequence

The power up sequence is designed to set up the DPU for either the read or write operation. Both these operations are executed by interrupt driven service routines. Figure 17 is the algorithm for the power up sequence. Step 1 is self-explanatory. Step 2 requires further explanation.

The circuitry that permits parallel I/O with the SBC 80/10(A) is two 8255 Programmable Peripheral Interface IC chips. The two chips provide 48 I/O lines organized in six 8-bit ports (1A, 1B, 1C, 2A, 2B and 2C). Depending on which of three modes of operation is chosen, these ports can be programmed for input, output, bidirectional data flow, or control ports through which external devices can gain access to the CPU. The simplest of the three is Mode 0. Step 2 programs the two 8255's in this mode.

Step 3 tests the read/write mode switch by loading the signal into the Carry flip-flop of the CPU. If "Write" is detected, that signal is used to initialize the 8-bit counter in the multiplexer and then is returned to the

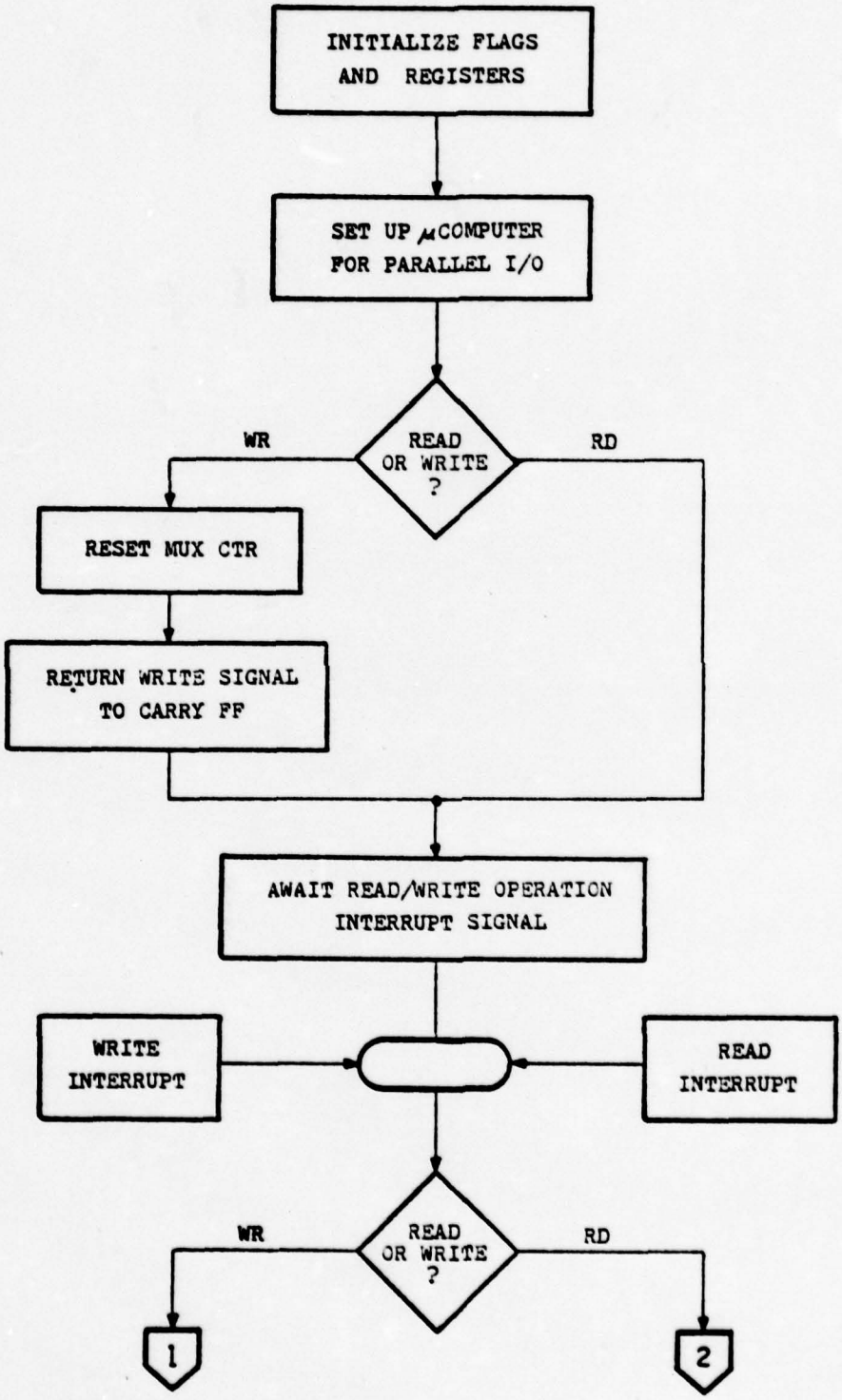



FIGURE 17 - POWER UP SEQUENCE ALGORITHM

Carry flip-flop. The program then suspends execution and awaits an interrupt signal. On the SBC 80/10(A) circuitry between the 8238 bus controller IC and the CPU is such that all interrupts, regardless of source, divert program flow to location $0038_{16}$. It is therefore necessary to check the read/write switch again and then proceed with the appropriate interrupt service routine.

2. Write Operation

The interrupt driving signal for the write operation is derived from the sample column LED. The signal is inverted so that its falling edge can be used to trigger the active low input to the 8080A's Interrupt line. In the power up sequence the counter in the multiplexer was reset. It cannot count, hence sample the interference pattern, until its associated flip-flop is reset. So the first step in the Write Operation Algorithm (Figure 18) is to enable the multiplexer's counter. This is done by sending a "1" to the K input of the enable/reset flip-flop. Each detector in the linear array is now gated open for a multiplexer clock period, $T_s$, of 2 ms. Half the clock period is allowed for the amplitude and phase detector channels to execute their functions. The CPU tests the multiplexer clock pulse and on the transition to the second half of $T_s$, commences A/D conversion of the analog data and stores it in memory. Loops 4 and 5 provide 44 μs needed by the analog I/O board for the A/D conversion.

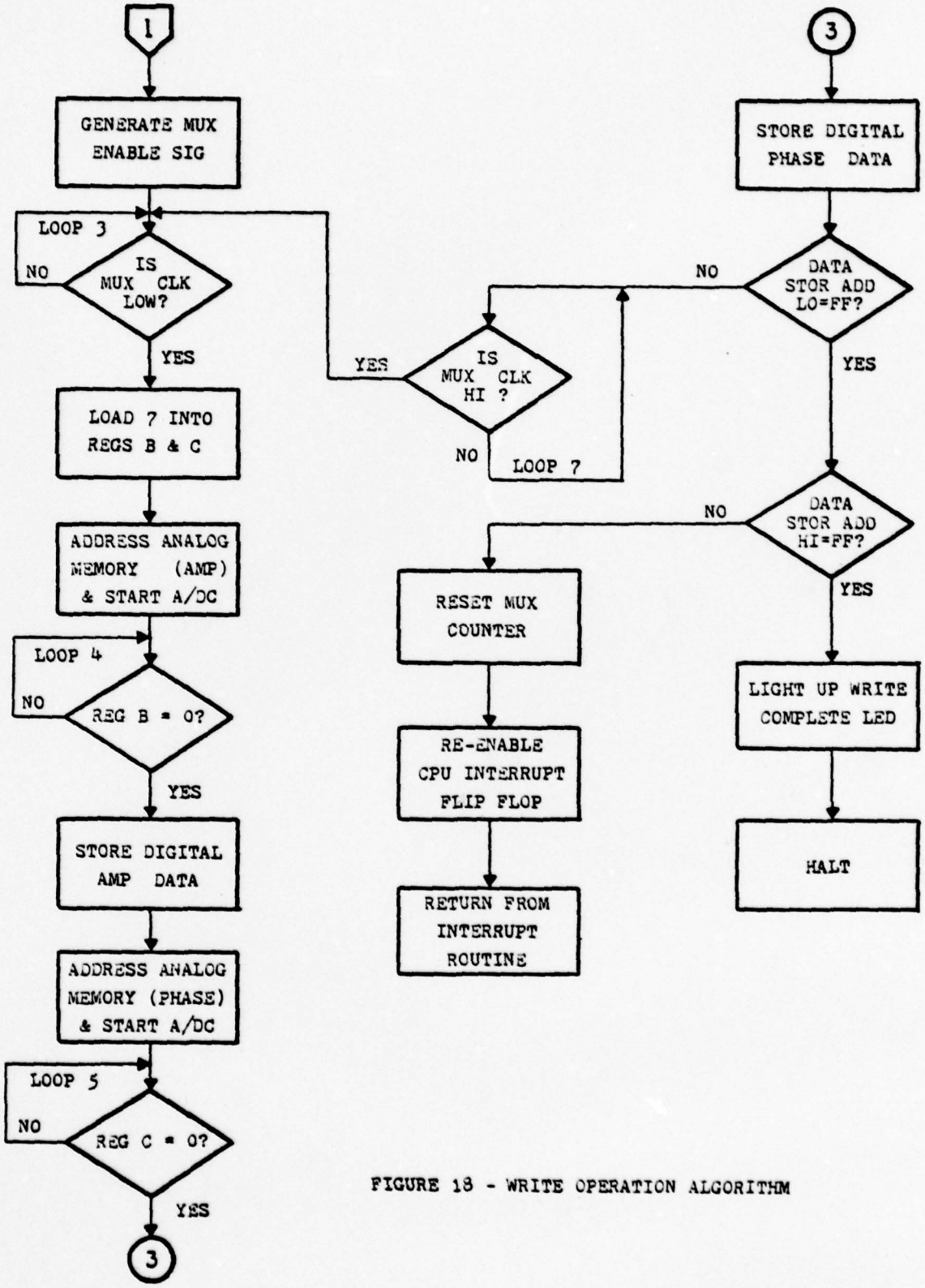



FIGURE 18 - WRITE OPERATION ALGORITHM

Loops 7 and 3 suspend DPU action until the second half of the next $T_s$ is sensed. This continues until one column of 128 samples has been taken, i.e., 256 data bytes have been stored. Next the number of sample columns taken is checked by examining the upper half of the data storage address. If the 128 columns have not been completed, the program executes the steps shown and returns from the interrupt routine to await the next sample column LED signal. If the sample matrix is complete, the program lights up an LED so indicating completion of the write operation. Figure 19 lays out a memory map for the DPU.

The bulk of the DPU was operational before arrival of the analog I/O board. A test program was written to check out the system thus far completed. Most of the program bugs were worked out using this program. Several small modifications to the test program and some additional debugging resulted in the preceding algorithm and program in Appendix F. In the test program, dummy data was loaded in a second PROM. Data was read from here and stored in the off board RAM. When first running this program on the Tektronix 8002 development system, no data was written to the off board RAM. Considerable review of hardware reference manuals for each of the DPU modules, software programs, and finally, consultation with factory engineers, revealed no clue as to the data transfer failure. One factory engineer suggested checking the address, data and

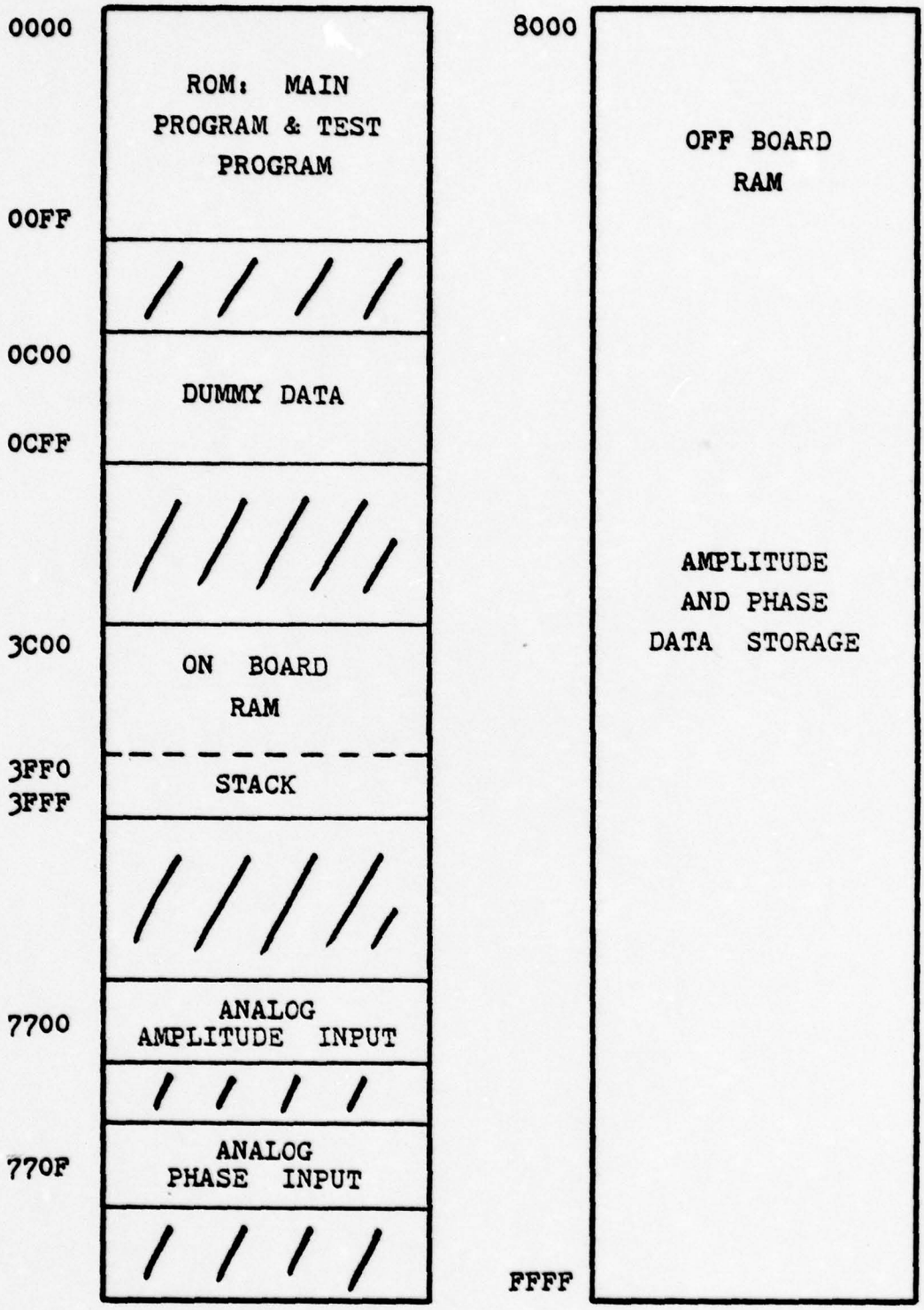



FIGURE 19 - DATA PROCESSING UNIT MEMORY MAP

control bus lines on an oscilloscope. To do this a short test program with a two instruction loop was written. The first instruction wrote a byte of dummy data to off board memory location $8000_{16}$. The second instruction jumped back to the write instruction. Address line 15 going high was used to trigger the oscilloscope. Sweep speed and trigger adjust were set to paint a steady picture of the signals input to a dual trace display. Next the handshaking signals that were supposed to be exchanged between the SBC 80/10(A) and the SBC 064 via the MULTIBUS were checked. The oscilloscope presented a replica of timing diagrams exactly as specified in hardware reference manuals. Next the address and data bus lines were checked with a probe from the scope. All lines checked out correctly. It was concluded the fault lay not in the writing operation. The above steps were repeated, only this time using a read instruction in place of the write instruction. Similar results were found. This was quite puzzling. It was decided to try the original test program again. This time when the contents of the off board RAM were checked, complete transfer of the dummy data had been successfully achieved. Pleasantly dumbfounded, the author concluded one of two things: either he had unwittingly uncovered and corrected a program bug, or the RAM board simply needed some warm up or burn in time. In the time it took to check the various signals and lines during the two short test

programs, the RAM board must have been written to and read from several billions of times. This may have been what was needed to get it functioning properly. The DPU may also have had a bad contact somewhere on one of the edge connectors.

When the analog I/O board finally arrived, it was seated into the SBC 604 Cardcage. Without the linear detector array to complete the integrated data acquisition system, analog values from the two detector channels were simulated with dc power sources, and the sample column LED signal was simulated with a pulser from a Digidesigner. With each press of the pulser, a sample column was taken. Between pulses the dc values were varied. Their digital equivalents were computed and compared with the data stored in the off board RAM. The results were successful.

3. Read Operation

Concurrent with this thesis effort was another thesis project whose objective was to record the data generated by the original system onto a cassette tape (Ref. 5). The cassette tape could then be transported to the PDP-11/50 computer for further processing. The ICT-WZ-2B2B Tape Recorder System from Datel is capable of recording data as fast as the original system could produce it. For the 128, or eventual 256, linear detector array scheme, however, it is much too slow. An interrupt routine was written to read stored data from the off board

RAM and transfer it to the cassette tape at the fastest speed the tape recorder could handle.

Three control signals must be exchanged between the DPU and the tape recorder. The first, a reset pulse to the tape recorder, is to insure the tape is set to the correct position to begin recording data. The reset pulse must be one millisec long. Since the CPU operates at much higher speeds than the recorder, it must test a status line from the recorder that indicates when it is ready to receive data. Once this status line tests true, the CPU must send a start pulse to the recorder.

Figure 20 presents the Read Operation Algorithm. Step 1 sets up a sample counter and a loop counter that will build a reset pulse 1 ms long. The tape recorder loads two 8-bit bytes of data at a time, so when the status line tests true, an amplitude and phase data pair is read out through Ports 2A and 2B. The CPU then provides a start pulse and the recorder writes the data onto the tape. The program continues this sequence until all sample data has been transferred. Data and control signals are sent back and forth between the DPU and recorder over an umbilical cord of 20 lines. This cord runs from the J1 and J2 ports of the SBC 80/10(A) to the J6 edge port of the tape recorder. Wire connections and descriptions are shown in Appendix E.

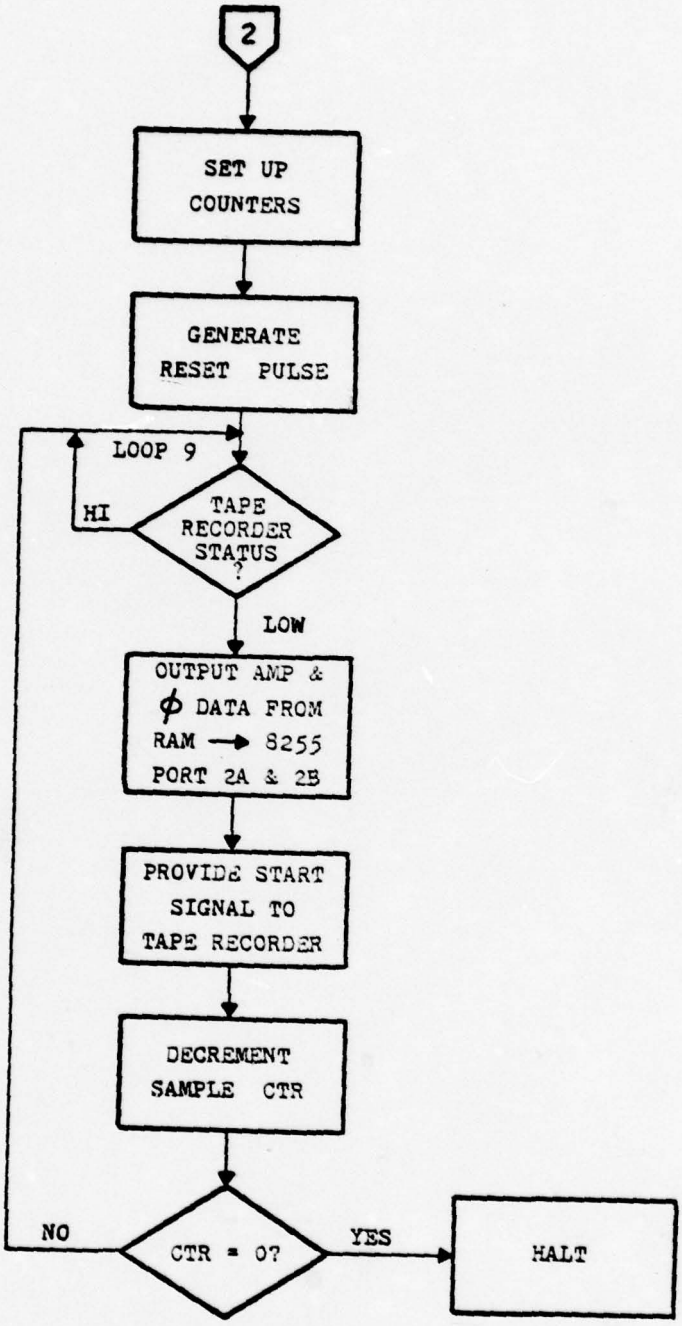



FIGURE 20 - READ OPERATION ALGORITHM

## VII. SUGGESTED FURTHER DEVELOPMENT OF SYSTEM

Completion of testing and design of the amplitude detection channel is the primary objective of further work. The objective was to expand the present system from a 128 detector scheme to a 256 detector scheme.

### A. SBC 80/10(A) EXPANDED ADDRESS/DATA/CONTROL BUS (EADCB)

A 256 square matrix generates 64K samples or 128K data bytes. A second RAM expansion board will be needed which can fit into the fourth slot of the SBC 604 Cardcage. Power provided by the SBC 635 can easily accommodate the fourth board. A problem arises with the address capability of the SBC 80/10(A). The MULTIBUS has 20 address lines and therefore the potential to address up to one megabyte of memory, but the SBC 80/10(A) can only address 64K memory cells. One answer is to replace the SBC 80/10(A) with the SBC 86/12, a 16 bit microcomputer from Intel with a 20 line address bus. That would cost $2140. Another answer is to modify the SBC 80/10(A)'s existing I/O structure to address a megabyte of memory. This explanation follows.

Within a one megabyte memory block, there are 16 blocks of 64K bytes each. Any one of these blocks can be assigned to an SBC 064 RAM expansion board by means of on board user selectable jumper connections. Multiple board systems (up to 16) can be assembled by assigning each board a different

block of 64K bytes. Once a RAM board has been jumper connected, it will answer to, i.e., be "enabled" by, any 20 bit address within its assigned 64K block. Conversely any 20 bit address outside the block will "disable" the board. Hence if multiple board systems are needed, board selection is accomplished merely by address selection.

Once a memory slot has been addressed, the SBC 80/10(A) must trigger an exchange with the SBC-064 by either a memory read or write command (MRDC/ or MWTC/ -- a "/" following a mnemonic means the signal is active low). Either of these two signals triggers a series of gated logic on the RAM board that ends with a transfer acknowledge (XACK/) signal being generated. This signal, when returned to the SBC 80/10(A), indicates that the data has been placed onto or accepted from the MULTIBUS data lines. How these "handshaking" signals are generated will be discussed later under Memory Write and Read Operations.

The first task is to "build" a 20 line address bus for the SBC 80/10(A) that addresses (and "selects") the RAM expansion board via the MULTIBUS. This can be done using the two 8255 Programmable Peripheral Interface IC chips described earlier. Mode 0 sets up the ports for straight input or output. Outputs are latched; inputs are not. Mode 1 programs two of the IC chip's three ports for either input or output, and the third port handles "handshaking" signals that control the I/O through those two ports.

Mode 2 sets up one port as an 8-bit bidirectional port. One port services handshaking signals for control of the bidirectional port on five of its lines. The other three can be used for general I/O. The third port can be set up for either input or output in either Mode 0 or Mode 1. On the SBC 80/10(A) only 8255 #1 can be operated in all three modes. 8255 #2 can only be programmed for Mode 0 operation.

The expanded address bus can be made using 20 of the I/O lines of 8255 #2 (ports 2A, 2B and 2C lower) programmed for output. Using a 50 pin edge connector with either wire wrap or solder leads, hard wire these outputs to the appropriate address pins of the SBC 604's MULTIBUS motherboard. A bidirectional data bus can be set up by programming 8255 #1 for Mode 2 and using Port 1A (the only port of the three with the bidirectional capability). Hard wired connections here are direct to the data lines of the MULTIBUS. Port 1C will provide the handshaking signals for exchange with the RAM board. Port 1B must be programmed for output, the reason for which will be discussed in the next section. Control bus connections will be discussed under memory read and write operations. When configured in this manner, the 8255 ports constitute a "peripheral" device that will share the use of the MULTIBUS for data transfer (see Figure 21). A distinction here between the system's external busses carried over the SBC-604's MULTIBUS

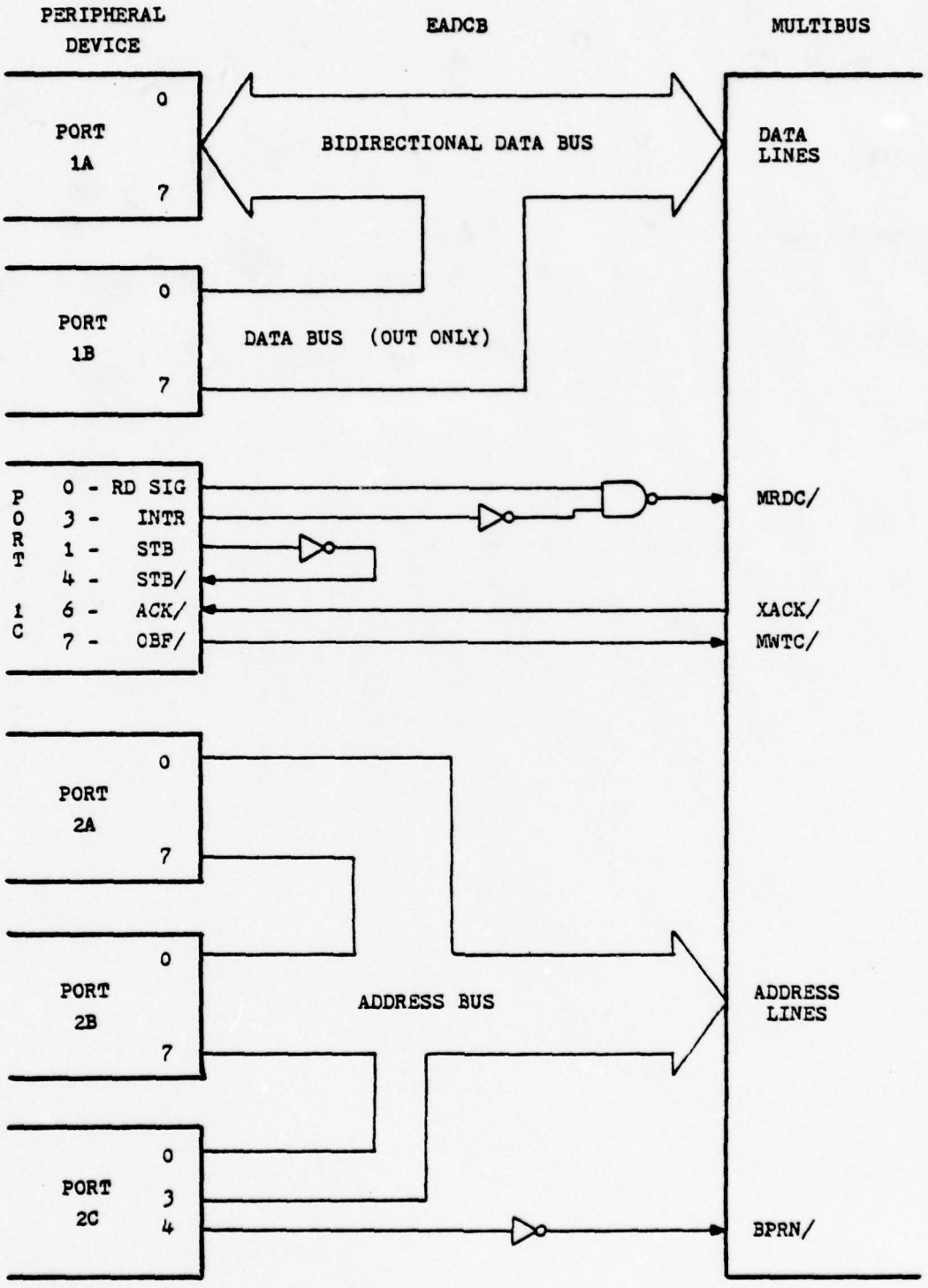


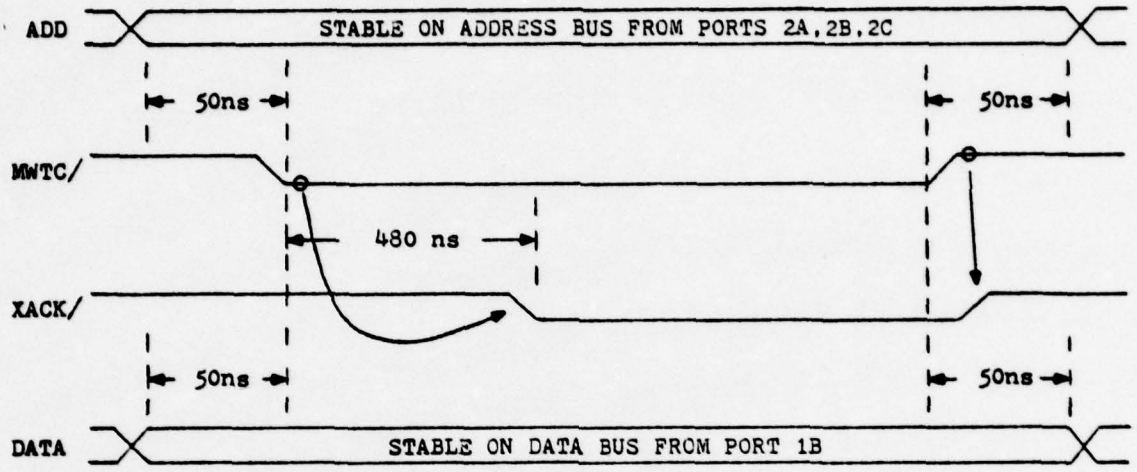

FIGURE 21 - EXPANDED ADDRESS/DATA/CONTROL BUS

motherboard and the internal busses on the SBC 80/10(A) board will become necessary shortly. Hereafter, reference to the external busses will be done using capital letters (e.g., ADDRESS BUS) and the internal busses using small case letters (e.g., data bus).

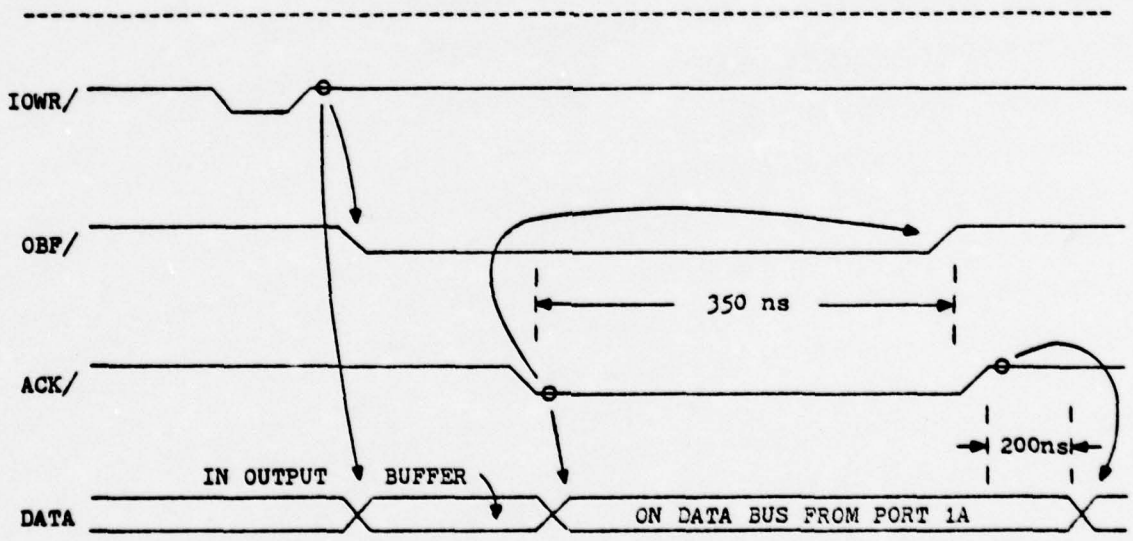
1. Memory Write Operation

The first step necessary in this operation is to write out the memory storage location to the ADDRESS BUS through 8255 #2 and the data out to the DATA BUS through Port 1B. These four ports must be programmed for Mode 0 operation. This simply latches the information into those ports and onto respective BUSSES. Concurrent with writing out the address, write a "1" to Port 2C-4. This must be inverted (there are unused inverting gates on the SBC-064) and input to Bus Priority IN (BPRN/) on the CONTROL BUS. This input isolates the SBC 80/10(A)'s internal busses from the system's external BUSSES. Now address and data information on the BUSSES will not be disturbed by further internal execution on the SBC 80/10(A) board.

Figure 22a portrays the timing necessary for writing data into the SBC-064. A MWTC/ command generated by the SBC 80/10(A) must be sent to the RAM board. The RAM board will respond with a XACK/ signal 480 ns later. MWTC/ setting high will trigger XACK/ to return high also. Note that the address location and data must be stable on their respective BUSSES a minimum of 50 ns before and after the MWTC/ command is issued and terminated. In Figure 22b,




(a) TIMING DIAGRAM FOR SBC 064




(b) TIMING DIAGRAM FOR 8255

FIGURE 22 - TIMING DIAGRAM FOR 256 DETECTOR SCHEME WRITE OPERATION

the timing diagram for the 8255 during output sequences is shown. When data is written out to Port 1A, it is latched into its output buffer. Loading this buffer resets the Output Buffer Full (OBF/ on Port 1C-7) low. Receipt of an active low acknowledge (ACK/ on Port 1C-6) will dump the data onto the output lines, i.e., the DATA BUS. Receipt of this signal will also set OBF/ high 350 ns later. When ACK/ sets high the output buffer in Port 1A will go into its high impedance state 200 ns later.

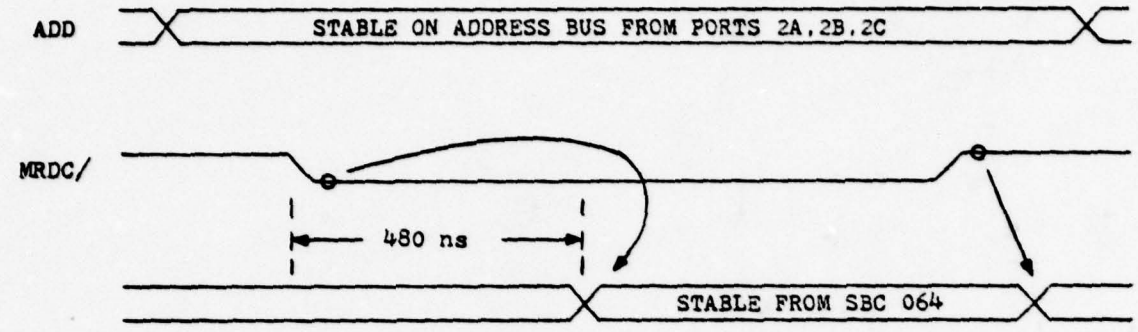
It is necessary to interconnect the two boards via the MULTIBUS so as to satisfy both these timing schemes. Note the similarity between the MWTC/ command required by the RAM board and the OBF/ signal issued by Port 1C-7 during an output sequence. Connect these two points together. Next note the similarity between the XACK/ signal returned by the RAM board and the ACK/ signal required by the 8255. Connect these two points together. Finally note that before any exchange of control signals occurs address and data information must be stable on their respective BUSSES for a minimum of 50 ns. This is accomplished by taking the first step described at the beginning of this section, i.e., writing this information out through Ports 2 and 1B, BEFORE the data is written out to Port 1A. With the above pair of connections made, the following sequence of control signals exchange now occurs. The output instruction executed by the CPU generates an IOWR/ signal. This sends data to the output buffer of

Port 1A and drops OBF/ low. The RAM board receives this low signal at its MWTC/ port, executes its logic and returns a XACK/ signal 480 ns later to the ACK/ port. When this signal is received OBF/ is set high 350 ns later. When OBF/ setting high is detected by the RAM board, it will set its XACK/ high, thus terminating the control signal exchange sequence. The limited time data is contributed through Port 1A is inconsequential. This completes the transfer of data from the SBC 80/10(A) to the RAM board over the EADCB.

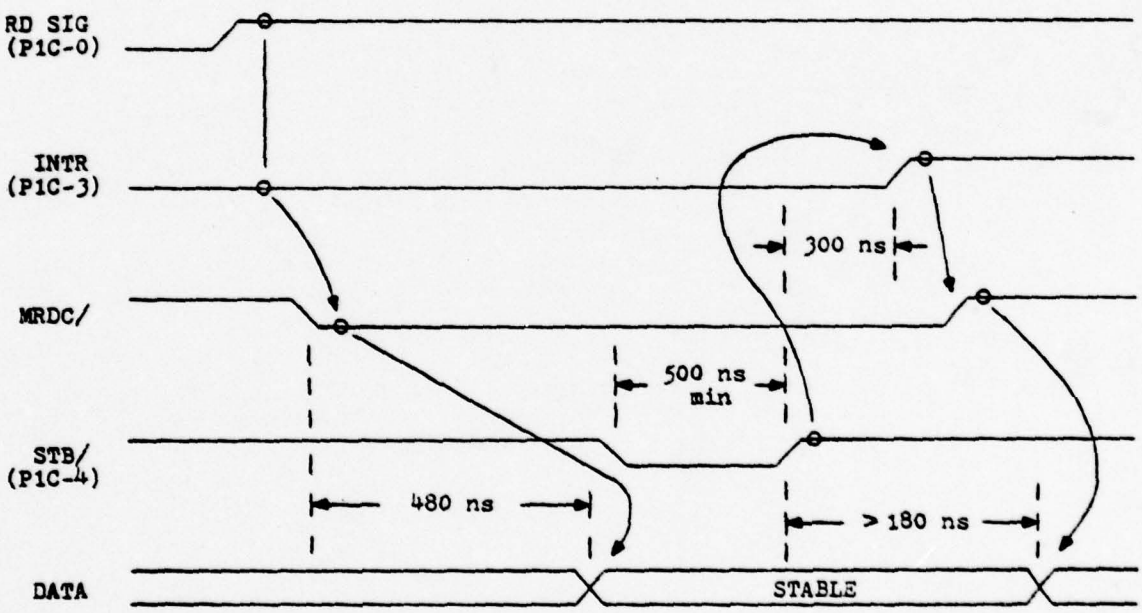
2. Memory Read Operation

The first step again is to write the address location onto the ADDRESS BUS through 8255 #2 and to isolate the internal bus from the external BUS. The next step is to generate a memory read command (MRDC/). This is done by wiring one of the general output lines from Port 1C (P1C-0) and the interrupt output line (P1C-3) inverted to the inputs of a NAND gate (see Figure 21). Unused inverting and NAND gates are available on the SBC-064. Since all "mask" flip-flops are reset during mode selection or device reset, the latch associated with Port 1C-0 will normally be low until purposely set. INTR is normally low until set by the rising edge of an active low pulse input to STB/ at Port 1C-4. So in the initial state MRDC/ will be high.

Figure 23 presents the timing diagrams for the RAM board and 8255 that must be matched for data transfer. To




(a) TIMING DIAGRAM FOR SBC 064




(b) TIMING DIAGRAM FOR 8255

FIGURE 23 - TIMING DIAGRAM FOR 256 DETECTOR SCHEME READ OPERATION

initiate the memory read sequence, set "Rd Sig" (P1C-0) high. The resulting low MRDC/ will trigger gated logic on the RAM board that will dump data from the memory cell addressed onto the DATA BUS 480 ns later. Then by wiring a second of the three general output lines of Port 1C (P1C-1) through an inverter to the STB/ line (P1C-4), an active low STB/ pulse can be sent to P1C-4 by writing a "1" to P1C-1. Then set STB/ high by writing a "0" to P1C-1. To strobe in data from the DATA BUS to Port 1A requires a minimum active low STB/ pulse of 500 ns duration and that data be held valid on the DATA BUS 180 ns following the rising edge of STB/. The time it takes the CPU to write first a "1", then a "0", to P1C-1 will yield an active low STB/ pulse well exceeding the minimum duration of 500 ns. The rising edge of STB/ will set the interrupt line 300 ns later. Recall that the inputs to the NAND gate were both high to generate a low MRDC/ signal. Now that INTR has been set high by the setting STB/ signal, the inverted INTR input to the NAND gate sets MRDC/ high again. This will in turn terminate valid data on the DATA BUS long after the data hold time of 180 ns required by the 8255.

With the data now latched into Port 1A, it must be loaded into the CPU. First reset Rd Sig to "0" (this will not affect MRDC/ because INTR is still high). Follow this with an INPUT instruction, which will send an IORD/ signal to the 8255. The falling edge of IORD/ will strobe the

data into the CPU and reset INTR (this will not affect MRDC/ because Rd Sig is now low). The off board memory read cycle is thus completed.

B. NOISE REDUCTION

The subject of noise reduction has never been addressed. It is anticipated the following noise sources will contaminate signal detection: (1) linear detector array, (2) preamplifiers between the array and multiplexer, (3) the multiplexer, (4) power splitter, and (5) preamplifiers in both detection channels. Using the ANZAC AM-110 amplifiers in some of the preamp stages compounds the noise problem because they are wide band, 0.5 to 100 MHz, amplifiers.

A cursory attempt to limit noise was made when testing the ANZAC amplifiers for their phase distortion characteristics. An LC tank circuit tuned to 1 MHz was placed in series with the two 30 dB amplifiers and then the frequency varied about 1 MHz. Some filtering action was noted when observing the output on an oscilloscope, but the skirts of the tank circuit's frequency response fell off much too gradually to be considered wholly effective. A high Q active band pass filter using multiple high slew rate operational amplifiers is recommended to achieve necessary noise elimination. Reference 6, Chapter 7 describes in detail the state variable active filter which offers a high Q band pass filter capable of operating at

high frequencies. These amplifiers will distort the phase -90°, but that would be another constant error source for which compensation could be made in software.

# VIII. CONCLUSIONS

Goals established at the outset of this thesis effort were achieved, on most counts, successfully. The data processing unit built around the SBC 80/10(A) microcomputer was able to receive and generate the necessary handshaking signals to control the multiplexer and process the data produced by the two detection channels. The 256 channel 2 level multiplexer proved equal to the task of passing sufficient numbers of cycles of each sample on to the detection channels. Although amplitude attenuation and phase distortion were detected, these error sources can be easily compensated for in software. The output of the phase detector was linear provided the input amplitudes of the detected and reference signals exceeded 15 dBV. Testing and evaluation of the amplitude detector fell short of completion due to component malfunction, however the limited testing conducted did yield results that confidently forecast satisfactory performance of this functional block in the overall system design.

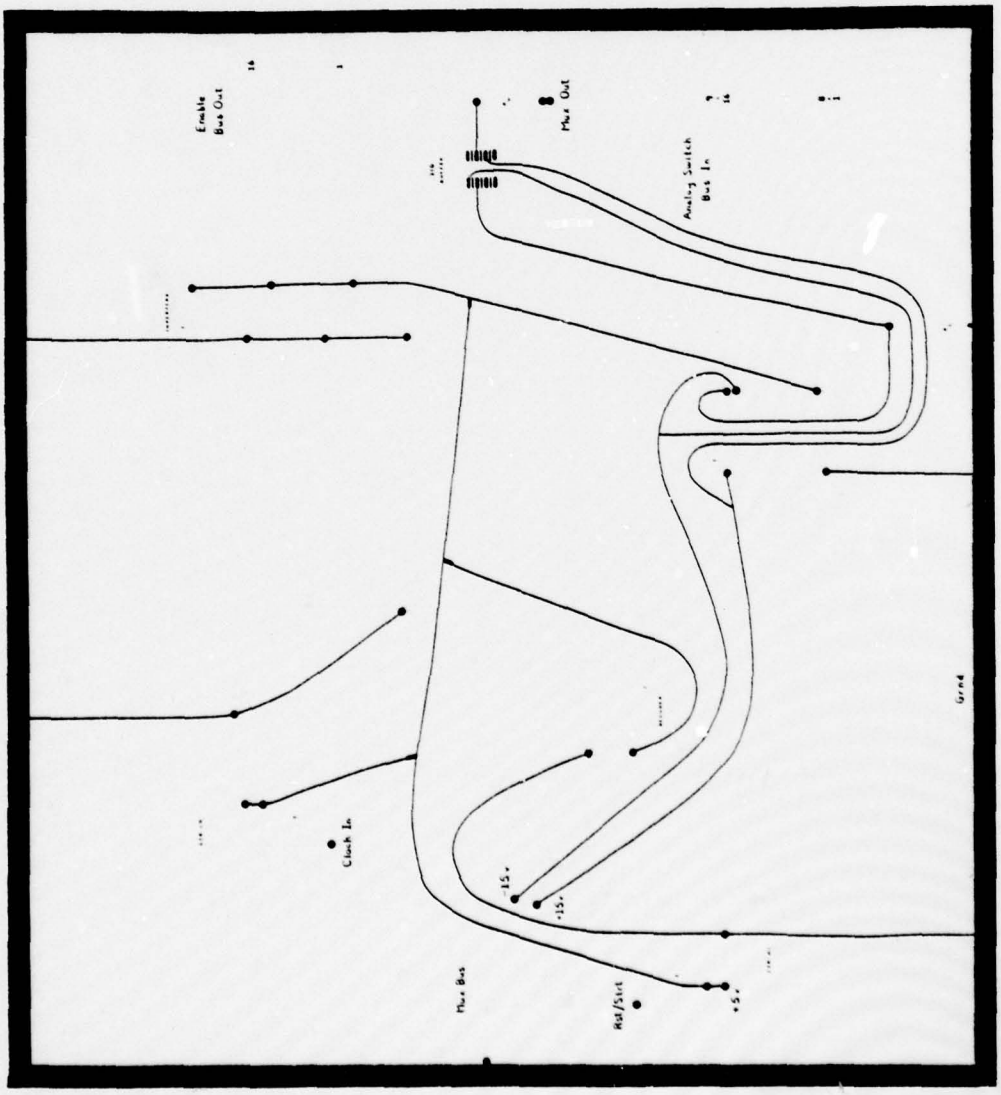
The components chosen in the design of this system offer a great deal of flexibility for expansion in several directions. The 128 detector scheme is easily expandable to the 256 detector scheme. The 16 input channels of the analog I/O board suggest even further expansion to a parallel detection channel scheme with four to eight pair

of amplitude and phase detectors. The only limiting factor would be the processing speed with which the DPU could handle the data generated. As suggested earlier, direct acoustic coupling to the PDP-11/50 computer at a 2300 baud rate will accomplish complete data transferral of a 256 square sample matrix in less than 11.5 minutes (allowing for start, stop and parity bits). Although not quite real time image processing, "expeditious" time image processing is a not too far distant reality.

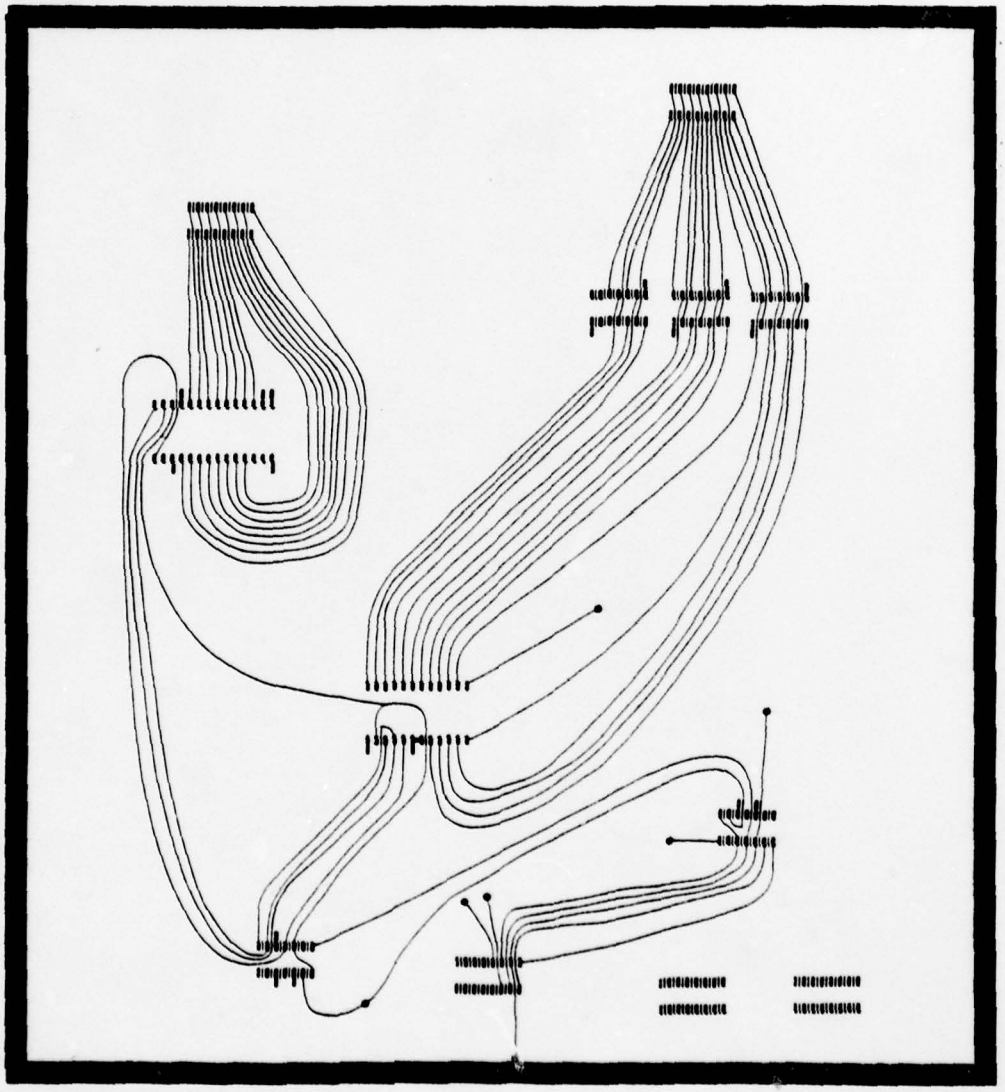
# APPENDIX A

## MULTIPLEXER PRINTED BOARD CIRCUIT DESIGNS

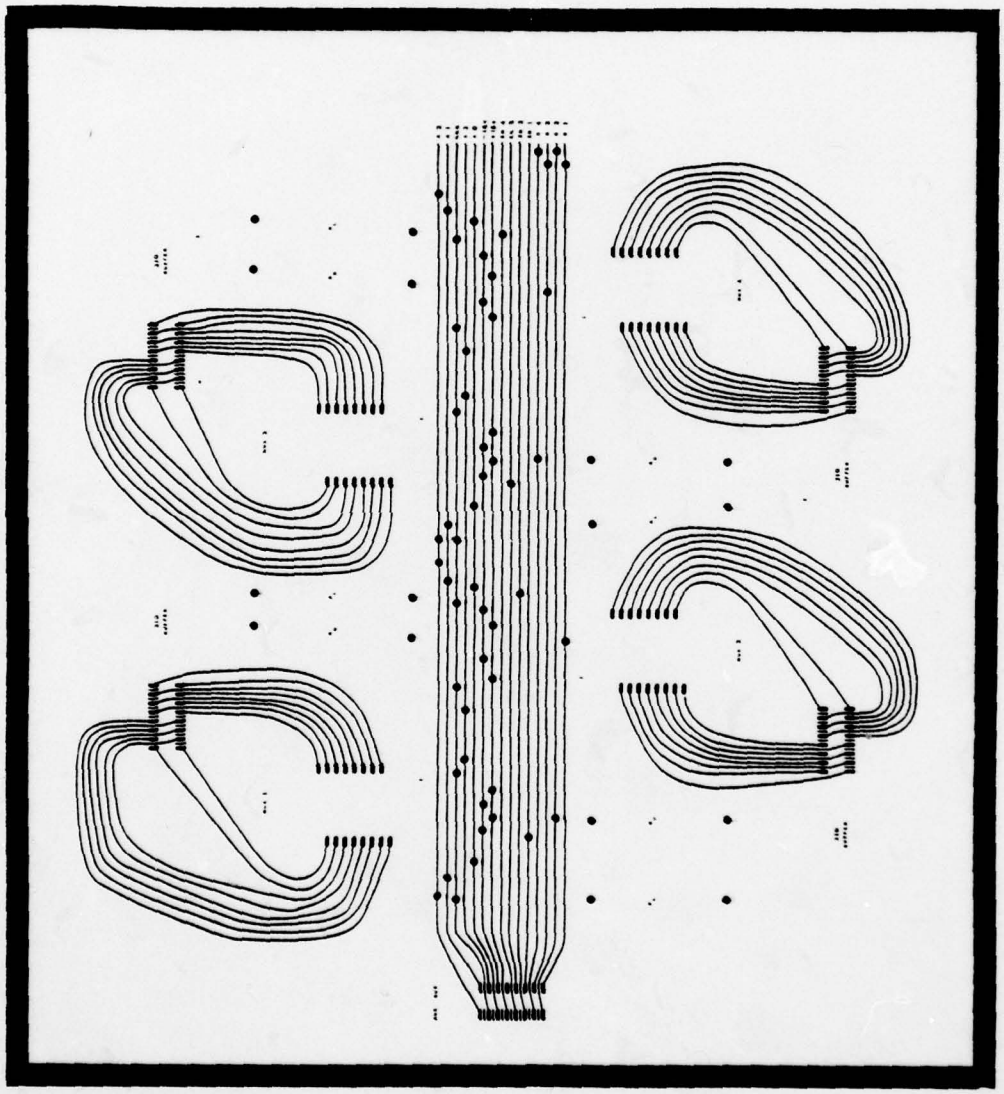
A two sided Master Board and 4 two sided 1st Level Input Boards make up the channel selection logic for the 256 channel 2 level analog multiplexer. A combined Reset/Enable and Clock logic board completes the design.



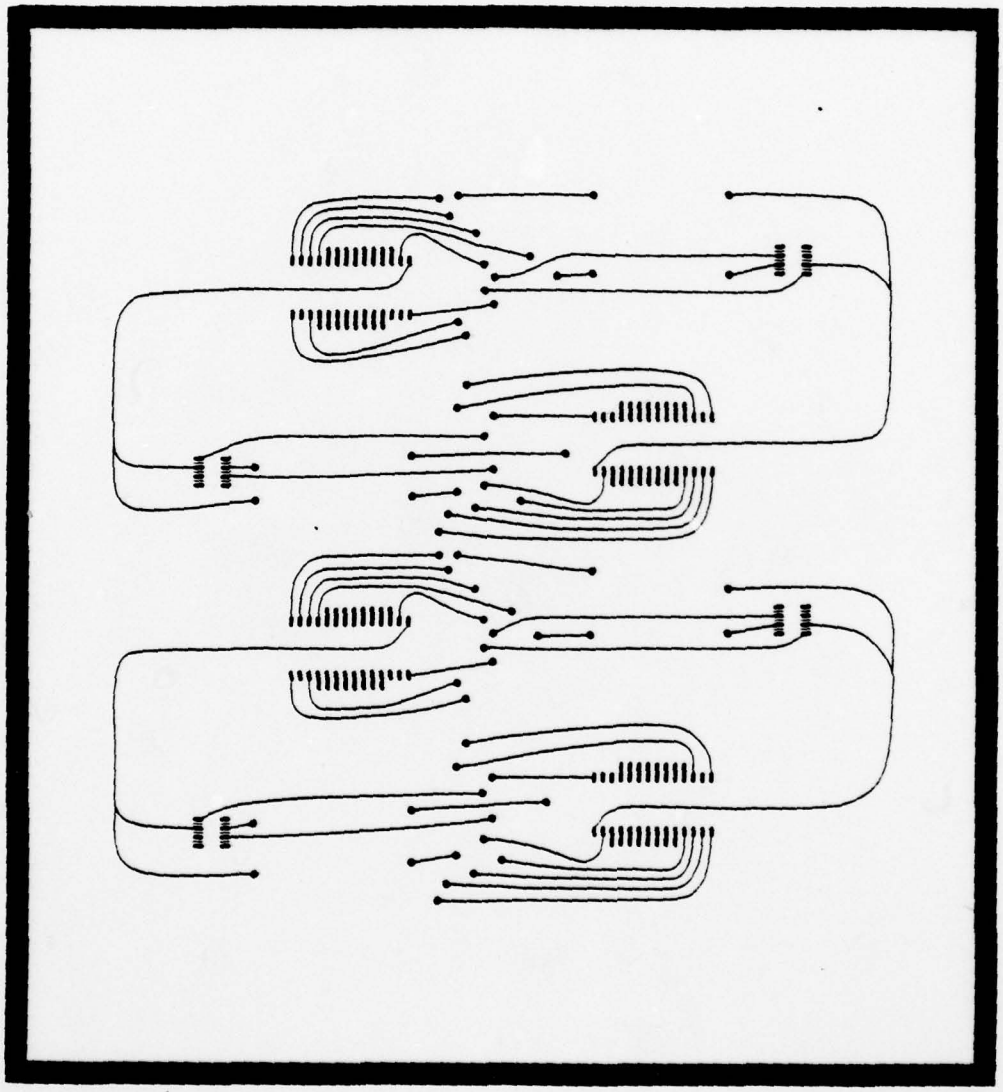

MASTER BOARD (Component side)



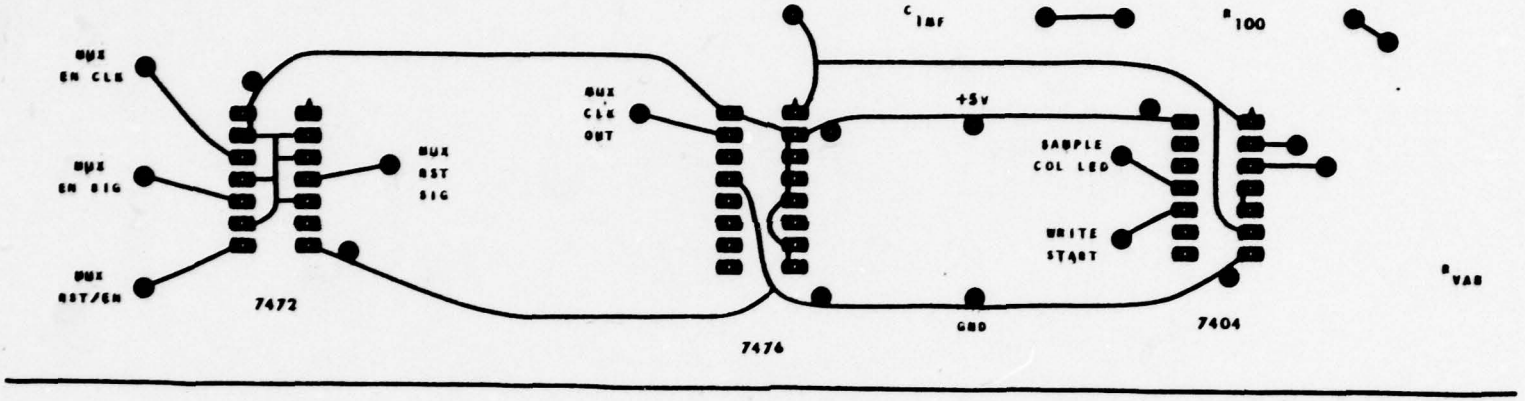
MASTER BOARD (Solder side)



1st LEVEL INPUT BOARD (Component side)



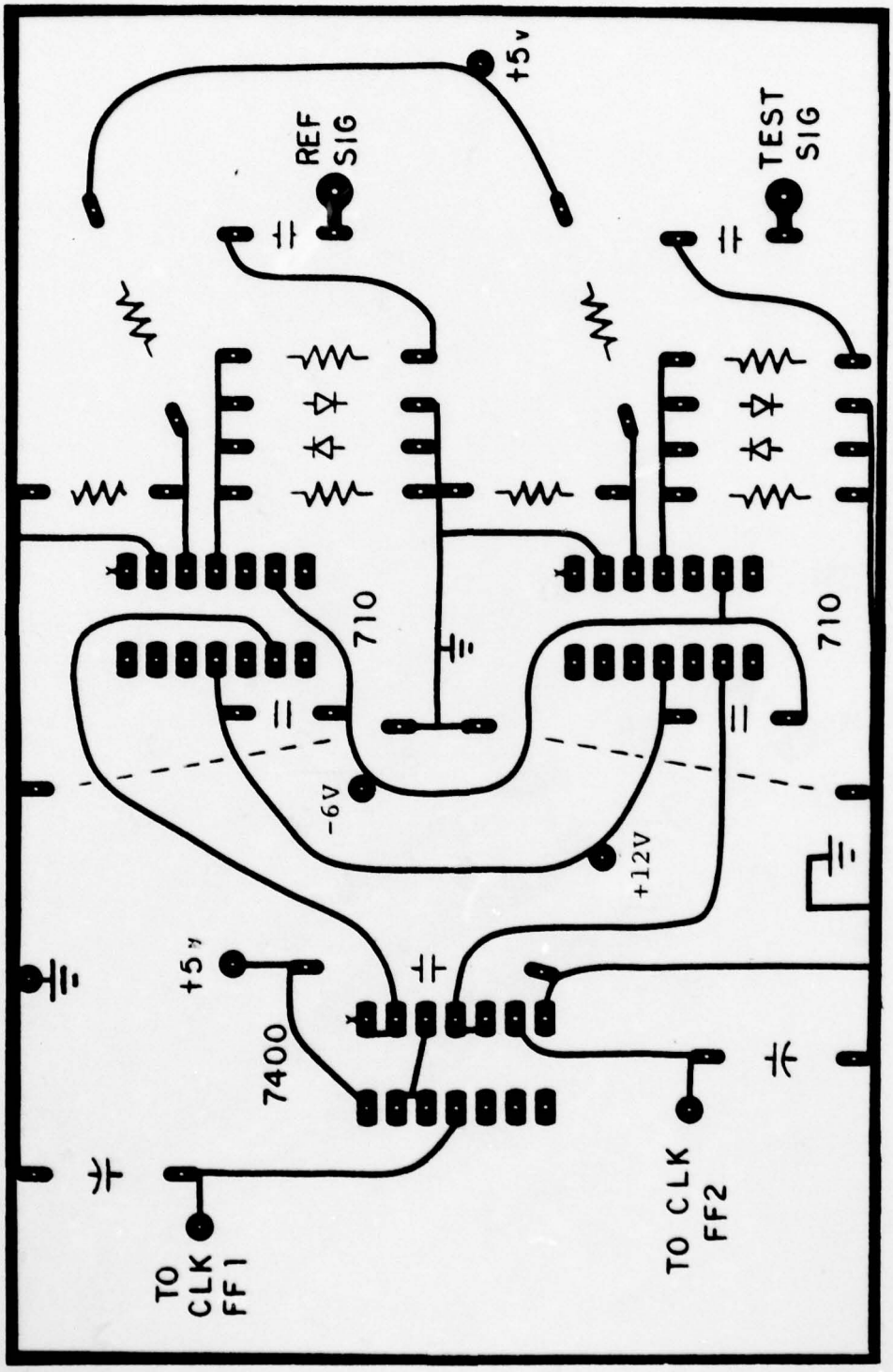
1st LEVEL INPUT BOARD (Solder side)



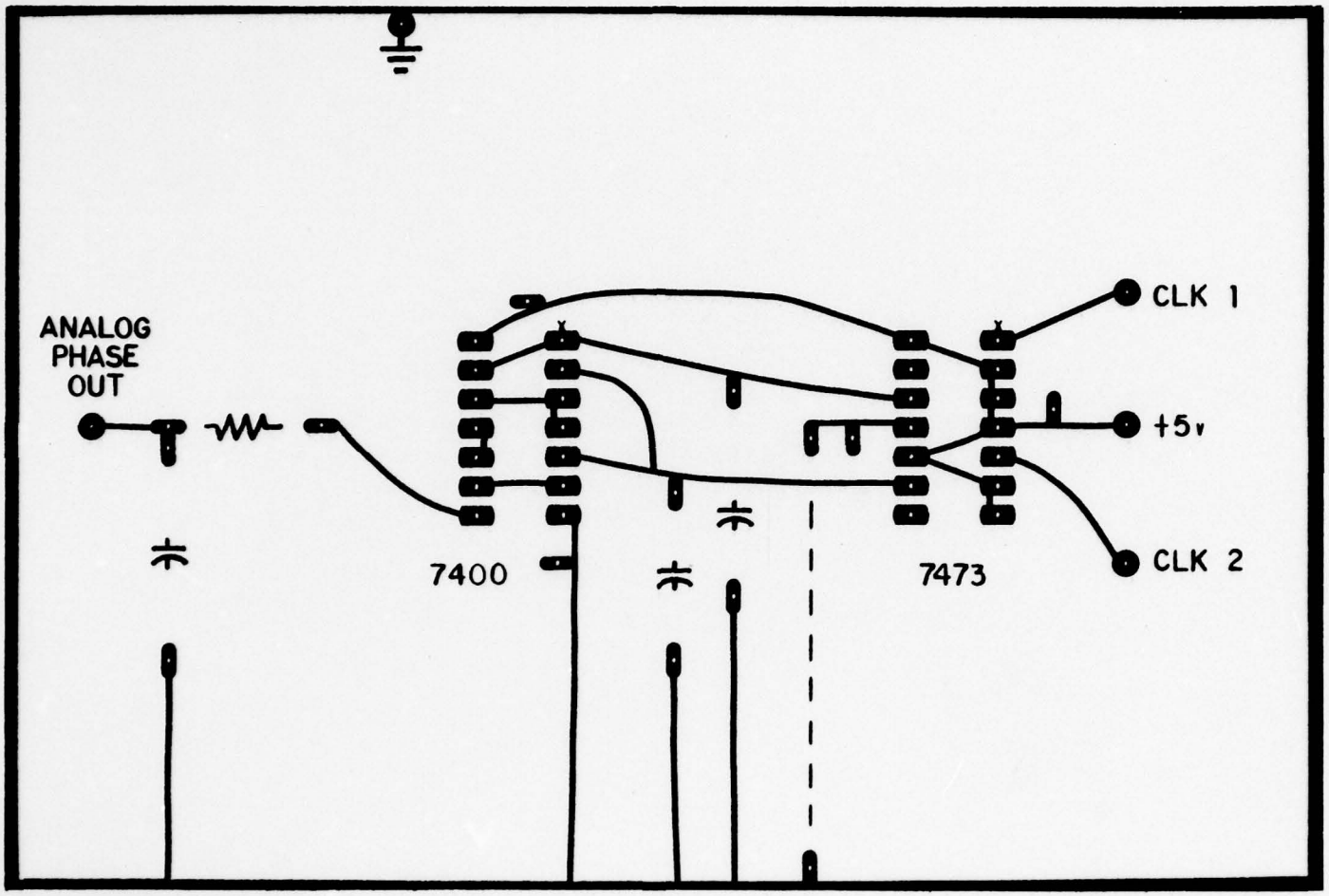

RESET/ENABLE and CLOCK LOGIC BOARD

APPENDIX B

PHASE DETECTOR PRINTED CIRCUIT BOARD DESIGNS

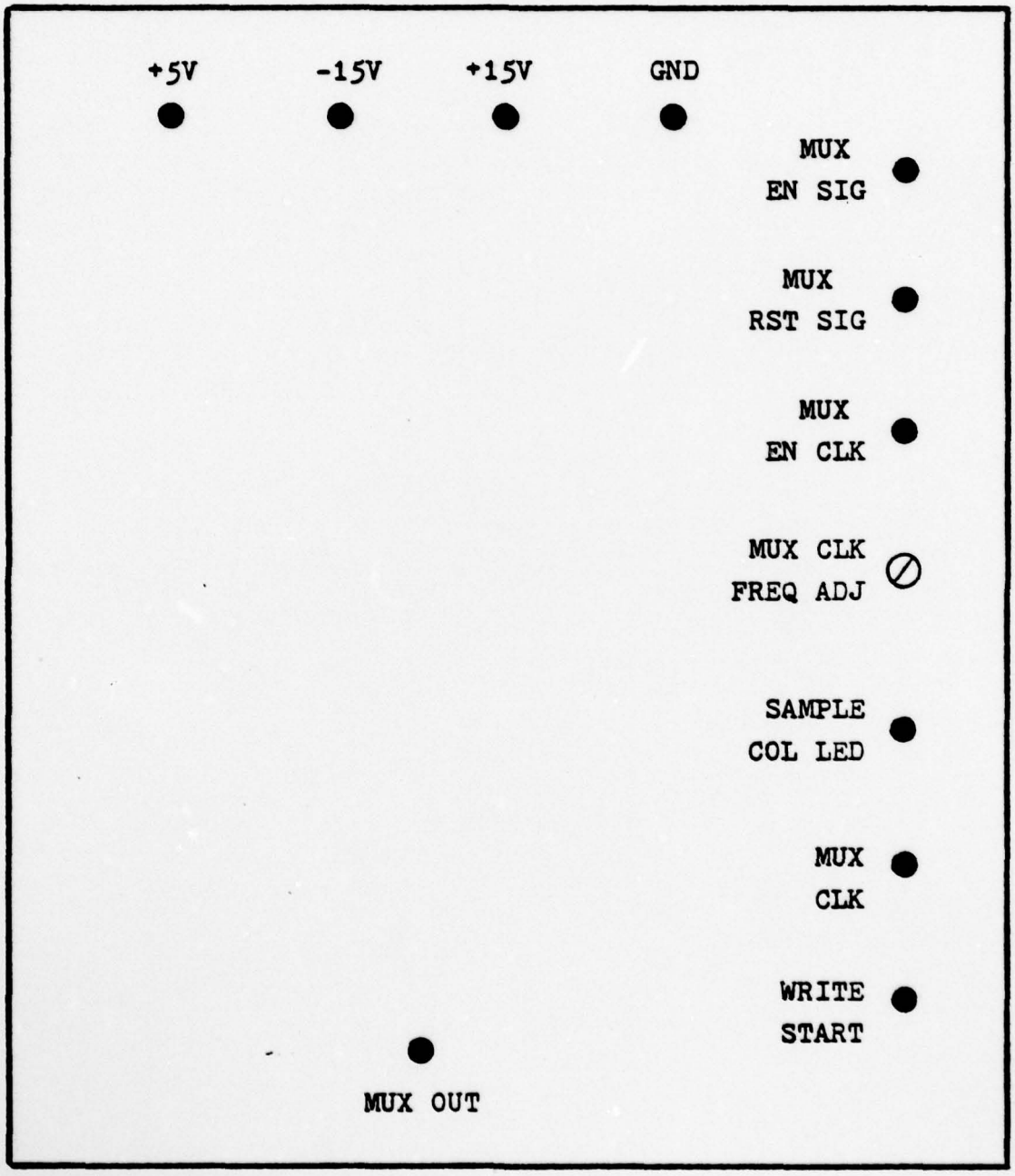



BOARD 1

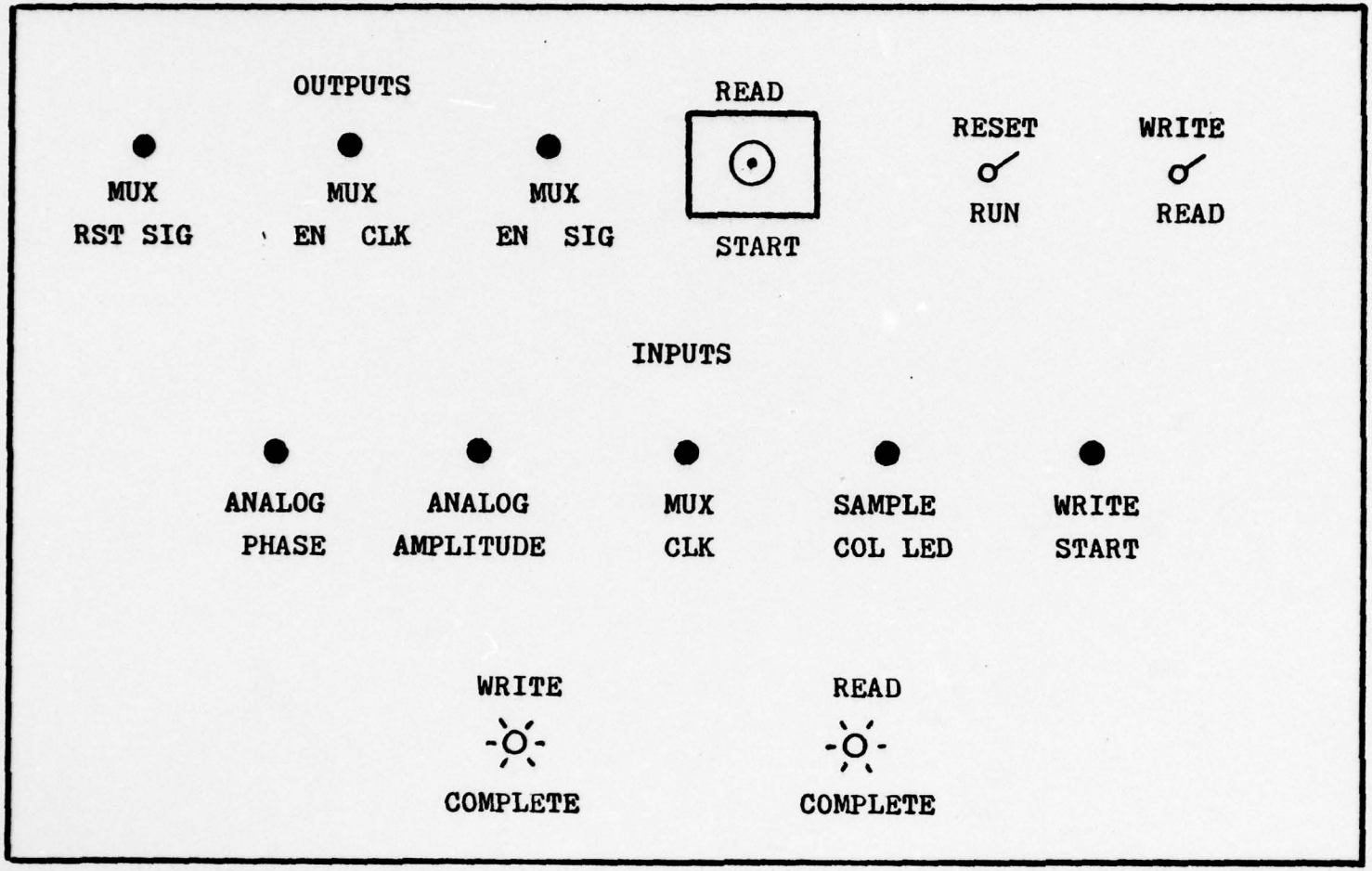



BOARD 2

APPENDIX C




MULTIPLEXER CONTROL PANEL DIAGRAM




DATA PROCESSING UNIT CONTROL PANEL DIAGRAM

## APPENDIX E

## DATA PROCESSING UNIT PORT CONNECTIONS

| Port P1 | Signal | To/From |
|---|---|---|
| 1-2 | Ground | MULTIBUS |
| 3-6 | +5 V | MULTIBUS |
| 7-8 | +12 V | MULTIBUS |
| 9-10 | -5 V | MULTIBUS |
| 11-12 | Ground | MULTIBUS |
| 13 | Bus Clock (9.21 MHz) | To Control Panel |
| 14 | System Reset | Fr Control Panel |
| 19 | Mem Rd Cmd | MULTIBUS |
| 20 | Mem Wr Cmd | MULTIBUS |
| 21 | I/O Rd Cmd | MULTIBUS |
| 22 | I/O Wr Cmd | MULTIBUS |
| 23 | Transfer Acknowledge | MULTIBUS |
| 28 | Address Line 17 | MULTIBUS |
| 30 | Address Line 18 | MULTIBUS |
| 32 | Address Line 19 | MULTIBUS |
| 34 | Address Line 20 | MULTIBUS |
| 42 | Read Start Interrupt | Fr Control Panel |
| 43-58 | Address Lines 0-15 | MULTIBUS |
| 59-74 | Data Lines 0-15 | MULTIBUS |
| 75-76 | Ground | MULTIBUS |
| 79-80 | -12 V | MULTIBUS |
| 81-84 | +5 V | MULTIBUS |
| 85-86 | Ground | MULTIBUS |

| Port P3 | Signal | To/From |
|---|---|---|
| 19 | Analog Amplitude | Fr Control Panel |
| 49 | Analog Phase | Fr Control Panel |

| Port J1 | Signal | To/From |
|---|---|---|
| 1 | Mux Enable | To Control Panel |
| 2 | Common Ground | To Muxer Ground |
| 3 | Read Complete LED | To Control Panel |
| 5 | Write Complete LED | To Control Panel |
| 7 | Mux Reset | To Control Panel |
| 33 | Mux Clock | Fr Control Panel |
| 35* | Tape Recorder Status | Fr Tape Recorder |
| 41 | Read/Write Mode | Fr Control Panel |
| 43 | Sample Column LED | Fr Control Panel |
| 49 | Write Start Interrupt | Fr Control Panel |

*Tape recorder status line comes from the Read Operation Umbilical Cord. It is solid brown in color.

| From Port J2 | Wire Description | Signal | To* Port J6 |
|---|---|---|---|
| 1 | Striped Black | Ground | 17 |
| 3 | Striped Green | $\phi$ Bit 3 | 12 |
| 5 | Striped Red | $\phi$ Bit 0 | 9 |
| 7 | White | $\phi$ Bit 1 | 10 |
| 9 | Striped Yellow | $\phi$ Bit 2 | 11 |
| 11 | Striped Purple | $\phi$ Bit 4 | 13 |
| 13 | Striped Blue | $\phi$ Bit 5 | 14 |
| 15 | Striped Orange | $\phi$ Bit 6 | 15 |
| 17 | Striped Gray | $\phi$ Bit 7 | 16 |
| 21 | Solid Blue | Start Pulse | 22 |
| 25 | Solid Yellow | Reset Pulse | 20 |
| 35 | Striped Gray | Amp Bit 7 | 8 |
| 37 | Striped Orange | Amp Bit 6 | 7 |
| 39 | Striped Blue | Amp Bit 5 | 6 |
| 41 | Striped Purple | Amp Bit 4 | 5 |
| 43 | Striped Red | Amp Bit 0 | 1 |
| 45 | White | Amp Bit 1 | 2 |
| 47 | Striped Yellow | Amp Bit 2 | 3 |
| 49 | Striped Green | Amp Bit 3 | 4 |
| **From Port J1** | | | |
| 35 | Solid Brown | Tape Status | 18 |

*Read Operation Umbilical Cord Connection from DPU to Tape Recorder

# APPENDIX F

## SBC 80/10(A) MICROCOMPUTER SOFTWARE

```
;-------------------------------------------------------------------------;
;                                                                         ;
;  THESIS PROGRAM FOR ACOUSTIC IMAGING SYSTEM              R.O. CARLOCK   ;
;  THESIS ADVISOR:                                          J.P. POWERS   ;
;                                                                         ;
;  THIS PROGRAM IS DESIGNED TO SIMULATE THE ACCESSION OF DATA FROM        ;
;  AMPLITUDE AND PHASE DETECTION CHANNELS OF AN ACOUSTIC IMAGING SYSTEM   ;
;  AND STORE IT IN ELECTRONIC MEMORY.  VARIABLE DC POWER LEVELS HAVE      ;
;  HAVE BEEN APPLIED TO TWO (2) MEMORY MAPPED ANALOG INPUT CHANNELS,      ;
;  M(7700) AND M(770F).  ANALOG TO DIGITAL CONVERSION IS ACCOMPLISHED,    ;
;  FOLLOWED BY DATA STORAGE IN AN OFF BOARD RAM EXPANSION MODULE.         ;
;  ONCE STORED IN MEMORY, THE READ OPERATION WILL TRANSFER THE DATA TO    ;
;  A CASSETTE TAPE FOR LATER PROCESSING BY THE PDP-11 COMPUTER.           ;
;                                                                         ;
;-------------------------------------------------------------------------;


;       ***   POWER UP SEQUENCE   ***

; INITIALIZE FLAGS AND REGISTERS

        ORG     0000H
        XRA     A       ; CLEAR ACC, CLEAR CARRY
        EI              ; ENABLE INTERRUPTS
        LXI     SP,3FFFH; ESTABLISH STACK AT M(3FFF)
        LXI     H,0FE83H; FE83 = DATA STORAGE ADDRESS CHECK BYTES >> REG HL
        LXI     D,7FFFH ; INITIALIZE DATA STORAGE ADDRESS

; SET UP MICROCOMPUTER FOR PARALLEL I/O

        LXI     B,1090H ; 1090 >> REG BC
        MOV     A,B     ; REG B = 10 >> ACC
        OUT     0EBH    ; SETS UP PORTS 2A, 2B AND 2C FOR MODE 0 OUTPUT
        MOV     A,C     ; REG C = 90 >> ACC
        OUT     0E7H    ; SETS UP PORT 1A FOR MODE 0 INPUT AND
                        ; PORT 1B FOR MODE 0 OUTPUT

; TEST FOR READ OR WRITE, SET UP AND AWAIT READ OR WRITE START INTERRUPT SIGNAL

        IN      0E4H    ; READ/WRITE SIGNAL >> PORT 1-A-1 >> ACC-1          (J1-41)
        RAR             ; ACC-1 >> ACC-0
        RAR             ; ACC-0 >> CARRY
        JNC     LOOP1   ; IF CARRY = 0, JUMP TO LOOP1
                        ; IF CARRY = 1, SET UP FOR WRITE OPERATION
        RAL             ; ROTATE CARRY = 1 BACK INTO ACC-0
        OUT     0E5H    ; SETS PORT 1-B-0 HIGH, RESETS MUX CTR              (J1-7)
        XRA     A       ; CLEARS ACC
        OUT     0E5H    ; RESETS PORT 1-B-0 LOW, MUX READY                  (J1-7)
        IN      0E4H    ; READ/WRITE SIGNAL >> PORT 1-A-1 >> ACC-1          (J1-41)
        RAR             ; ACC-1 >> ACC-0
        RAR             ; ACC-0 >> CARRY
LOOP1   NOP             ; MICROCOMPUTER AWAITS MANUAL INTERRUPT THAT
                        ; INITIATES THE READ OR WRITE OPERATION
        JMP     LOOP1   ;
        NOP             ;
        NOP             ; INTERRUPT WILL RESTART PROGRAM AT M(0038).
        NOP             ; NOP(S) FILL IN INTERVENING LOCATIONS.
        NOP             ;
        NOP             ;
        NOP             ;
        JNC     READ    ; IF CARRY = 0, JUMP TO READ OPERATION
                        ; IF CARRY = 1, CONTINUE WITH WRITE OPERATION
```

```
;       ***   WRITE OPERATION   ***

; GENERATE MUX ENABLE PULSE

        XRA     A       ; CLEAR ACC
        ORI     08H     ; LOADS "1" >> ACC-3
        OUT     0E5H    ; ACC-3 = 1 >> PORT 1-B-3 >> MUX ENABLE              (J1-1)
        XRA     A       ; CLEAR ACC
        OUT     0E5H    ; TERMINATE MUX ENABLE PULSE

LOOP3   IN      0E4H    ; MUX CLK >> PORT 1-A-7 >> ACC-7                     (J1-33)
        RAL             ; ACC-7 >> CARRY
        JC      LOOP3   ; IF MUX CLK (INVERTED) HIGH, RETURN TO LOOP3; O/W CONTINUE

; LOAD ANALOG AMPLITUDE FROM M(7700) & ANALOG PHASE FROM M(770F)

        LXI     B,0707H ; SETS UP REGISTERS B AND C AS COUNTERS FOR TIMING
                        ; LOOPS THAT ALLOW THE ANALOG I/O BOARD TIME FOR A/D
                        ; CONVERSION OF AMPLITUDE AND PHASE DATA
        LDA     7700H   ; ACCESSES ANALOG AMPLITUDE DATA AT M(7700)
                        ; AND COMMENCES A/D CONVERSION
LOOP4   DCR     B       ; LOOP4 PROVIDES 44 MICROSECONDS NEEDED FOR A/D CONVERSION
        JNZ     LOOP4   ;
        LDA     7700H   ; DIGITAL AMPLITUDE DATA >> ACC
        INX     D       ; INCREMENT REG DE
        STAX    D       ; ACC = AMPLITUDE DATA >> M(REG DE)
        LDA     770FH   ; ACCESSES ANALOG PHASE DATA AT M(770F)
                        ; AND COMMENCES A/D CONVERSION
LOOP5   DCR     C       ; LOOP5 PROVIDES 44 MICROSECONDS NEEDED FOR A/D CONVERSION
        JNZ     LOOP5   ;
        LDA     770FH   ; DIGITAL PHASE DATA >> ACC
        INX     D       ; INCREMENT REG DE
        STAX    D       ; ACC = PHASE DATA >> M(REG DE)

; CHECK DATA STORAGE ADDRESS

        MOV     A,H     ; REG H = FE >> ACC
        CMP     E       ; IS ACC = FE < REG E?
        JNC     LOOP7   ; IF NO, GO TO LOOP7
        CMC             ; IF YES, CLEAR CARRY
        MOV     A,L     ; REG L = 83 >> ACC
        CMP     D       ; IS ACC = 83 < REG D?
        JNC     SKIP1   ; IF NO, RESET MUX COUNTER
        XRA     A       ; IF YES, CLEAR ACC
        ORI     02H     ; LOADS "1" >> ACC-1
        OUT     0E5H    ; ACC-1 = 1 >> PORT 1-B-1.  LIGHTS UP WRITE COMPLETE LED
        HLT             ; HALT

; RESET MUX COUNTER AND HOLD

SKIP1   XRA     A       ; CLEAR ACC
        ORI     01H     ; LOADS "1" >> ACC-0
        OUT     0E5H    ; ACC-0 = 1 >> PORT 1-B-0 >> RESET MUX CTR           (J1-7)
        XRA     A       ; CLEAR ACC
        OUT     0E5H    ; ACC-0 = 0 >> PORT 1-B-0 >> MUX READY              (J1-7)

; ENABLE INTERRUPT FOR THE NEXT SAMPLE COLUMN

LOOP6   IN      0E4H    ; NEW COLUMN INPUT = WRITE INTERRUPT SIG >> ACC-0    (J1-43)
        RAR             ; ACC-0 >> CARRY
        JNC     LOOP6   ; IF WRITE INTERRUPT (INVERTED) LOW, RETURN TO LOOP6
        NOP             ; ALLOW INTERRUPT LOW-HIGH TRANSITION SETTLING TIME
        EI              ; ENABLE INTERRUPT
        NOP             ; ALLOW INTERRUPT TO ENABLE
        RET             ; RETURN FROM WRITE INTERRUPT SERVICE ROUTINE

LOOP7   IN      0E4H    ; INPUT MUX CLK >> PORT 1-A-7 >> ACC-7               (J1-33)
        RAL             ; ACC-7 >> CARRY
        JNC     LOOP7   ; IF MUX CLK (INVERTED) LOW, RETURN TO LOOP7
        JMP     LOOP3   ; IF MUX CLK (INVERTED) HIGH, RETURN TO LOOP3
```

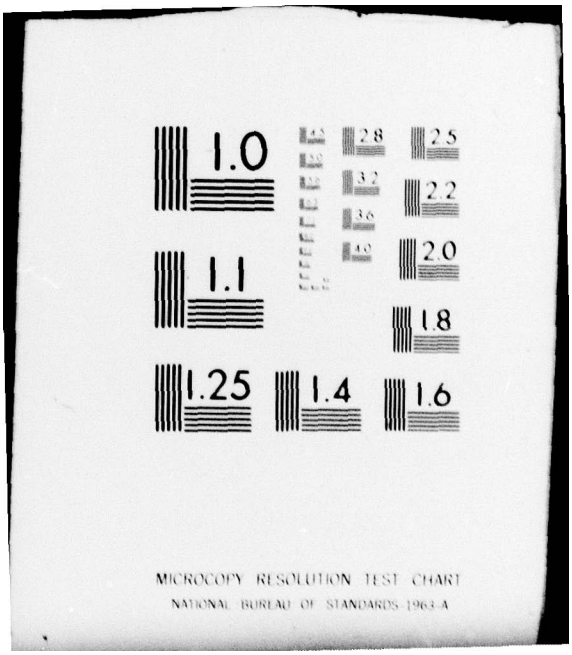
```
;       ***   READ OPERATION   ***

READ    LXI     B,407FH ; (1) SETS UP  RESET LOOP COUNTER (REG B).   16
                        ;     MICROSEC/LOOP FOR 64 LOOPS WILL GENERATE A
                        ;     RESET PULSE FOR 1 MILLISEC.
                        ; (2) SETS UP DATA TRANSFER COMPLETE COUNTER (REG C)
                        ;     TO COUNT 128 SAMPLES

; RESET PULSE GENERATION

LOOP8   ORI     0FFH    ; LOADS "1" >> ACC-0
        OUT     0EAH    ; ACC-0 = 1 >> PORT 2-C-0                          (J2-25)
        DCR     B       ; REG B - 1 >> REG B
        JNZ     LOOP8   ; IF REG B NOT = 0, RETURN TO LOOP8
        ORI     0FEH    ; LOADS "0" >> ACC-0
        OUT     0EAH    ; TERMINATE  RESET PULSE

; STATUS CHECK

LOOP9   IN      0E4H    ; TAPE RECORDER STATUS >> PORT 1-A-6               (J1-35)
        RAL             ; ACC-6 >> ACC-7
        RAL             ; ACC-7 >> CARRY
        JNC     LOOP9   ; IF STATUS (INVERTED) LOW, RETURN TO LOOP9; O/W CONTINUE

; OUTPUT AMPLITUDE AND PHASE DATA TO PORTS 2A AND 2B

        INX     D       ; INCREMENT DATA STORAGE ADDRESS
        LDAX    D       ; M(REG DE) = AMPLITUDE DATA >> ACC
        OUT     0E8H    ; ACC = AMPLITUDE DATA >> PORT 2A
        INX     D       ; INCREMENT DATA STORAGE ADDRESS
        LDAX    D       ; M(REG DE) = PHASE DATA >> ACC
        OUT     0E9H    ; ACC = PHASE DATA >> PORT 2B

; PROVIDE START PULSE TO TAPE RECORDER

        ORI     0FFH    ; 1111 1111 >> ACC
        ANI     0FAH    ; LOADS "0" >> ACC-2
        OUT     0EAH    ; ACC-2 = 0 >> PORT 2-C-2                          (J2-21)
        NOP             ; PUTS OUT 2 MICROSEC START PULSE
        ORI     0FEH    ; LOADS "1" >> ACC-2
        OUT     0EAH    ; TERMINATES START PULSE

; CHECK # OF SAMPLES TAKEN

        DCR     C       ; REG C - 1 >> REG C
        JNZ     LOOP8   ; IF REG C NOT = 0, RETURN TO LOOP8
        XRA     A       ; CLEAR ACC
        ORI     04H     ; LOADS "1" >> ACC-2
        OUT     0E5H    ; ACC-2 = 1 >> PORT 1-B-2.  LIGHTS UP READ COMPLETE LED
        HLT             ; HALT
        END
```

AD-A074 446 NAVAL POSTGRADUATE SCHOOL MONTEREY CA F/G 9/2
ANALOG AND DIGITAL HARDWARE DEVELOPMENT FOR A MICROCOMPUTER CON--ETC(U)
JUN 79 R O CARLOCK

UNCLASSIFIED NL

2 OF 2
AD A074446

END
DATE FILMED
10-79
DDC


1.0
1.1
1.25
1.4
1.6
2.8
3.2
3.6
4.0
2.5
2.2
2.0
1.8
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

## LIST OF REFERENCES


1. Patton, J.W., A Hardware Design for a Computer Aided Acoustic Imaging System, M.S.E.E. Thesis, Naval Postgraduate School, 1977.

2. De Blois, J.R.Y., An Improved Hardware Design for a Computer Aided Acoustic Imaging System, M.S.A.S. Thesis, Naval Postgraduate School, 1977.

3. Culpepper, J.C., Analog to Digital Conversion and Hardware Improvement for a Computer Aided Acoustic Imaging System, M.S.E.E. Thesis, Naval Postgraduate School, 1978.

4. Electronics Circuit Designer's Casebook, p. 38, Electronics, McGraw-Hill.

5. Colton, R.A., Microcomputer Based Digital Data Acquisition Controller, M.S.E.E. Thesis, Naval Postgraduate School, 1979.

6. Lancaster, D.E., Active Filter Cookbook, 1st ed., p. 156-165, Howard W. Sams & Co., Inc., 1976.

## INITIAL DISTRIBUTION LIST

| | | No. Copies |
|---|---|---|
| 1. | Defense Documentation Center<br>Cameron Station<br>Alexandria, Virginia 22314 | 2 |
| 2. | Library, Code 0142<br>Naval Postgraduate School<br>Monterey, California 93940 | 2 |
| 3. | Department Chairman, Code 62<br>Department of Electrical Engineering<br>Naval Postgraduate School<br>Monterey, California 93940 | 1 |
| 4. | Assoc. Professor John P. Powers, Code 62Po<br>Department of Electrical Engineering<br>Naval Postgraduate School<br>Monterey, California 93940 | 2 |
| 5. | Professor Rudolf Panholzer, Code 62Pz<br>Department of Electrical Engineering<br>Naval Postgraduate School<br>Monterey, California 93940 | 1 |
| 6. | Major Reid O. Carlock, USMC<br>United States Naval Academy<br>Annapolis, Maryland 21402 | 2 |
| 7. | Dr. Gary Hutton<br>Central Institute for Industrial Research<br>Forskningsv. 1, Oslo 3, Norway | 1 |
| 8. | Mr. Norman Caplan<br>Automation, Bioengineering and Sensing<br>Systems Program<br>National Science Foundation<br>1800 G Street<br>Washington, D.C. 20550 | 2 |